LC72121MA

PLL Frequency Synthesizer for Electronic Tuning

ON Semiconductor®

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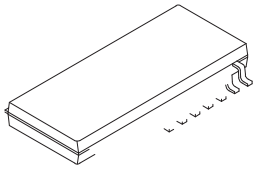
Overview

The LC72121MA are high input sensitivity (20 mVrms@130 MHz) PLL frequency synthesizers for 3 V systems. These ICs are serial data (CCB*) compatible with the LC72131K/KMA, and feature the [illegible] An MOS transistor for an active low-pass filter is built in.



I/O ports

Output-only ports: 4 pins

I/O ports: 2 pins

Supports the output of a clock time base signal.

Serial data I/O

Support CCB* format communication with the system controller.

Operating ranges

Supply voltage : 2.7 to 3.6 V

Operating temperature : 40 to +85°C

Package

MFP24SJ (300 mil)

*

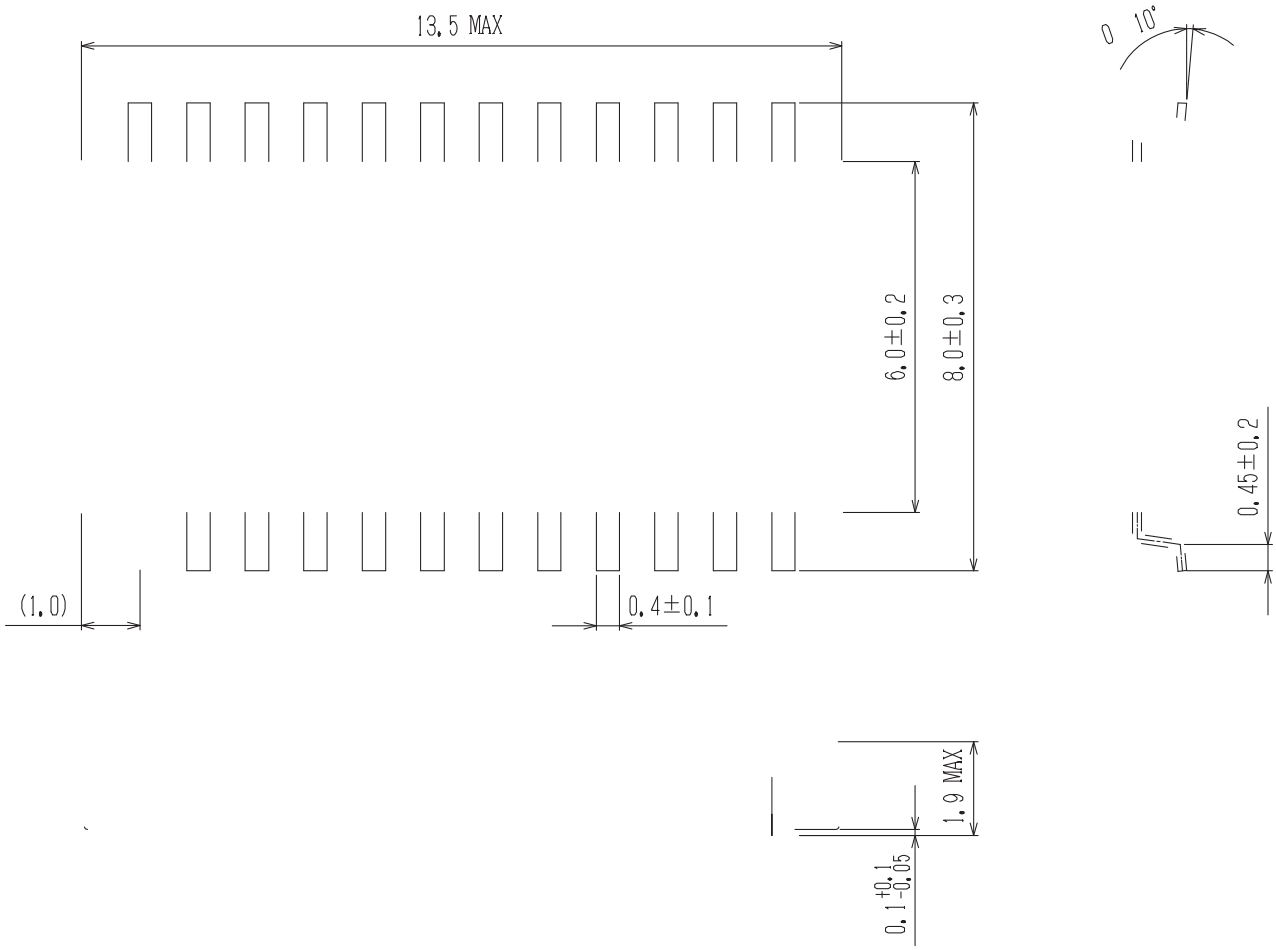
ORDERING INFORMATION

Specifications

Absolute Maximum Ratings

Package Dimensions

SOIC24W / MFP24SJ (300 mil)



Pin Assignment

Block Diagram

Continued from preceding page.

Procedures for Input and Output of Serial Data

This product uses the CCB (Computer Control Bus), which is Ours audio product serial bus format, for data input and output. This product adopts an 8-bit address CCB format.

Structure of the DI Control Data (serial data input)

[1] IN1 mode

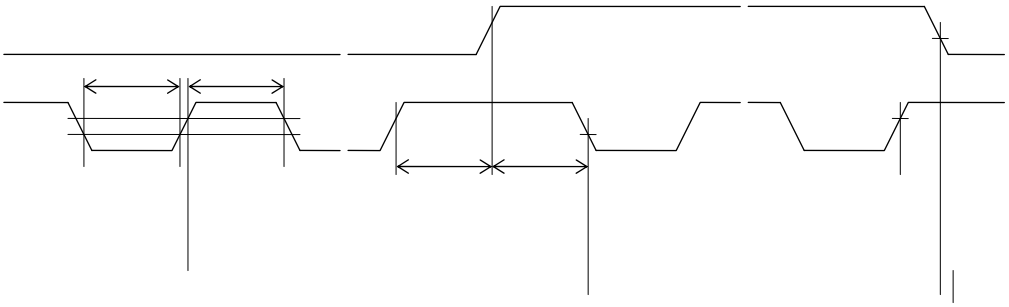
[2] IN2 mode

Control Data

1.Serial Data Input (IN1/IN2) t_{SU}, t_{HD}, t_{ES}, t_{EH}, 0.75 s t_{LC} 0.75 s

(1) CL: Normally high

Serial Data Timing



Structure of the Programmable Divider

Structure of the IF Counter

The LC72121MA IF counter is a 20-bit binary counter, and takes the IF signal from the IFIN pin as its input. The result of the count can be read out serially, MSB first, from the DO pin.

The IF frequency (Fc) is measured by determining how many pulses were input to the IF counter in the stipulated measurement time, GT.

$$Fc = \frac{C}{GT} \quad (C=Fc$$

IF Counter Operation

Applications must first, before starting an IF count operation reset the IF counter by setting CTE in the serial data to 0. The IF counter operation is started setting CTE in the serial data from 0 to 1. Although the serial data is latched by dropping the CE pin from high to low, the IF signal input to the IFIN pin must be provided within the wait time from the point CE goes low. Next, the readout of the IF counter after measurement is complete must be performed while CTE is still 1, since the counter will be reset if CTE is set to 0.

Note: If IF counting is used, applications must determine whether or not the IF IC SD (station detect) signal is present in the microcontroller software, and perform the IF count only if that signal is asserted. This is because auto-search techniques that use IF counting only are subject to incorrect stopping at points where there is no station due to IF buffer leakage.
Note that the LC72121MA input sensitivity can be controlled with the IFS bit in the serial data. Reduced sensitivity mode (IFS = 0) must be selected when this IC is used in conjunction with an IF IC that does not provide an SD output and auto-search is implemented using only IF counting.

IFIN Minimum Sensitivity Standard

Unlocked State Detection

Unlocked state detection is performed during the reference frequency (fref) period (interval). This means that a period at least as long as the period of the reference frequency is required to recognize the locked/unlocked state. However, applications must wait at least twice the period of the reference frequency immediately after changing the divisor (N) before checking the locked/unlocked state.

At the point of data output 1 in figure 3, the unlocked state data will indicate the unlocked state, since the VCO frequency is not stable (locked) yet. In cases such as this, the application should wait at least one whole period and then check again whether or not the frequency has stabilized with the data output 2 operation in the figure. Applications can implement even more reliable recognition of the locked state by performing several more checks of

Clock Time Base Usage Notes

When using the clock time base output function, the output pin ($\overline{BO1}$) pull-up resistor must have a value of over 100k . The use of a Schmitt input in the microcontroller that accepts this signal is recommended to reduce chattering. This is to prevent degradation of the VCO C/N characteristics when combining with a loop filter that uses the internal transistor provided to form a low-pass filter. Although the ground for the clock time base output pin (V_{SSd}) and the ground for the transistor (V_{SSa}) are isolated internally on the chip, applications must take care to avoid ground loops and minimize current fluctuations in the time base pin to prevent degradation of the low-pass filter characteristics.

Other Items

(1) Notes on the phase comparator dead zone

When the charge pump is used with one of the ON/ON modes, correction pulses are generated from the charge pump even if the PLL is locked. As a result, it is easy for the loop to become unstable, and special care is required in application design. The following problems can occur if an ON/ON mode is used.

(1) Sidebands may be created by reference frequency leakage.
(2) Sidebands may be created by low-frequency leakage due to the correction pulse envelope.

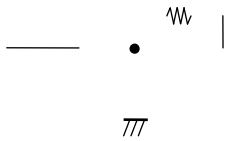
Although the loop is more stable when a dead zone is present (i.e. when an OFF/OFF mode is used), a dead zone makes it more difficult to achieve excellent C/N characteristics. On the other hand, while it is easy to achieve good C/N characteristics when there is no dead zone, achieving good loop stability is difficult. Accordingly, the DZA and DZB settings, in which there is no dead zone, can be effective in situations where a signal-to-noise ratio of 90 to 100dB or higher is required in FM reception, or where it is desirable to increase the pilot margin in AM stereo

Dead Zone

As shown in figure 1, the phase comparator compares a reference frequency (fr) with fp. As shown in figure 2, the phase comparator's characteristics consist of an output vo

(7) Front end connection example

Since this product is designed with the relatively high resistance of 200k for the pulldown (on) resistors built in to the FMIN and AMIN pins, a common AM/FM local oscillator buffer can be used as shown in the following circuit.



(8) PD pin

Note that the charge pump output voltage is reduced when this IC, which is a 3-V system, is used to replace the LC72131K/KMA, which is a 5-V system. This means that since the loop gain is reduced, the loop filter constants, the lock time (SD wait time), and other related parameters must be reevaluated in the end product design.

Pin States after a Power on Reset