LC72131K, LC72131KMA

PLL Frequency Synthesizer for Tuners in Radio/Cassette Players

ON Semiconductor®

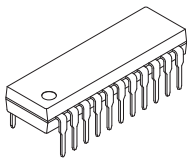
www.onsemi.com

Overview

The LC72131K and LC72131KMA are PLL frequency synthesizers for use in tuners in radio/cassette players.
They allow high-performance AM/FM tuners to be implemented easily.

Features

- High speed programmable dividers
  - FMIN: 10 to 160 MHz····· pulse swallower (built-in divide-by-two prescaler)
  - AMIN: 2 to 40 MHz ····· pulse swallower
  - 0.5 to 10 MHz ····· direct division
- IF counter
  - IFIN: 0.4 to 12 MHz ····· AM/FM IF counter
- Reference frequencies
  - Twelve selectable frequencies (4.5 or 7.2 MHz crystal)
  - 100, 50, 25, 15, 12.5, 6.25, 3.125, 10, 9, 5, 3, 1 kHz
- Phase comparator
  - Dead zone control
  - Unlock detection circuit
  - Deadlock clear circuit
  - Built-in MOS transistor for forming an active low-pass filter
- I/O ports
  - Dedicated output ports: 4
  - Input or output ports: 2
  - Support clock time base output
- Serial data I/O
  - Support CCB* format communication with the system controller.
- Operating ranges
  - Supply voltage : 4.5 to 5.5 V
  - Operating temperature : 40 to +85 C
- Packages
  - LC72131K : DIP22S (300mil)
  - LC72131KMA : MFP20J (300mil)



PDIP22 / DIP22S (300 mil)
[LC72131K]

SOIC20W / MFP20J (300 mil)
[LC72131KMA]

* Computer Control Bus (CCB) is an ON Semiconductor's original bus format and the bus addresses are controlled by ON Semiconductor.

ORDERING INFORMATION

See detailed ordering and shipping information on page 23 of this data sheet.

Specifications

Absolute Maximum Ratings at Ta = 25 C, V_{SS} = 0 V

Parameter	Symbol	Pins	Conditions	Ratings	Unit
Supply voltage	V_{DD} max	V_{DD}		0.3 to +7.0	V
Maximum input voltage	V_{IN}1 max	CE, CL, DI, AIN		0.3 to +7.0	V
	V_{IN}2 max	XIN, FMIN, AMIN, IFIN		0.3 to V_{DD}+0.3	V
	V_{IN}3 max	$\overline{IO1}$, $\overline{IO2}$		0.3 to +15	V
Maximum output voltage	V_O1 max	DO		0.3 to +7.0	V
	V_O2 max	XOUT, PD		0.3 to V_{DD}+0.3	V
	V_O3 max	$\overline{BO1}$ to $\overline{BO4}$, $\overline{IO1}$, $\overline{IO2}$, AOUT		0.3 to +15	V
Maximum output current	I_O1 max	$\overline{BO1}$		0 to 3.0	mA
	I_O2 max	DO, AOUT		0 to 6.0	mA
	I_O3 max	$\overline{BO2}$ to $\overline{BO4}$, $\overline{IO1}$, $\overline{IO2}$		0 to 10	mA
Allowable power dissipation	Pd max		Ta 85 C [LC72131K]	350	mW
			Ta 85 C [LC72131KMA]	180	mW
Operating temperature	Topr			40 to +85	C
Storage temperature	Tstg			55 to +125	C

Note 1: Power pins V_{DD} and V_{SS}: Insert a capacitor with a capacitance of 2,000pF or higher between these pins when using the IC.

Allowable Operating Ranges at Ta = 40 C to +85 C, V_{SS} = 0 V

Parameter	Symbol	Pins	Conditions	Ratings			unit
				min	typ	max	
Supply voltage	V_{DD}	V_{DD}		4.5		5.5	V

Note 1: Recommended crystal oscillator CI values:
CI 120 Ω (For a 4.5 MHz crystal)
CI 70 Ω (For a 7.2 MHz crystal)
The characteristics of the oscillation circuit depends on the printed circuit board, circuit constants, and other factors. Therefore we recommend consulting with the anufacturer of the crystal for evaluation and reliability.
Note 2: Refer to "Serial Data Timing".

Electrical Characteristics in the Allowable Operating Ranges

Parameter	Symbol	Pins	Conditions	Ratings			unit
				min	typ	max	
Built-in feedback resistance	Rf1	XIN			1.0		MΩ 1.4 ref466.86 657.

Package Dimensions
unit : mm

[LC72131K]

Package Dimensions
unit : mm

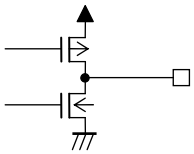
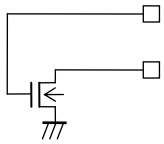
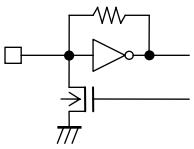
[LC72131KMA]

SOIC20W / MFP20J (300 mil)
CASE 751DE
ISSUE O

Pin Functions

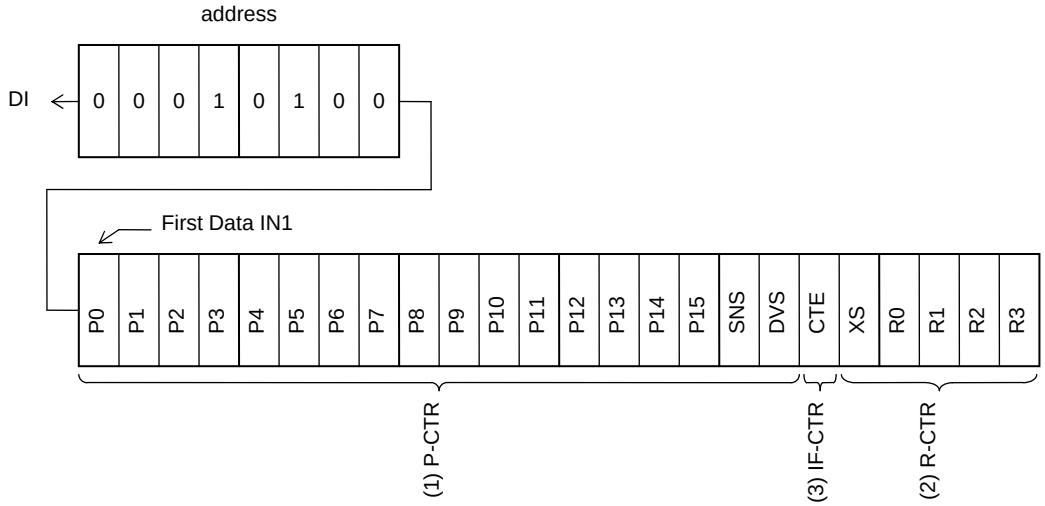
Symbol	Pin No.		Type	Functions	Circuit configuration
	LC72131K	LC72131KMA			
XIN	1				
XOUT					

Continued from preceding page.

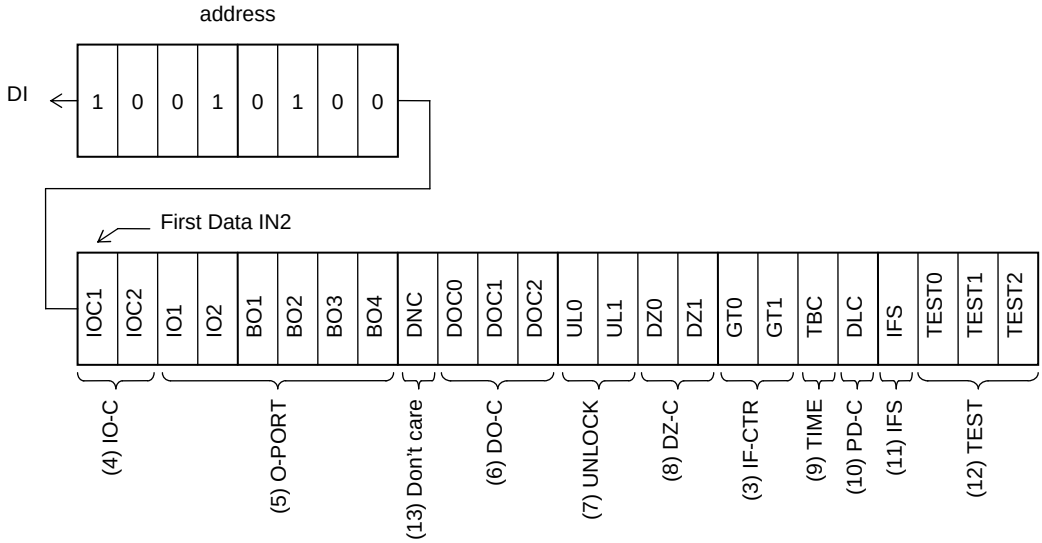
Symbol	Pin No.		Type	Functions	Circuit configuration
	LC72131K	LC72131KMA			
PD	18	16	Charge pump output	PLL charge pump output When the frequency generated by dividing the local oscillator frequency by N is higher than the reference frequency, a high level is output from the PD pin. Similarly, when that frequency is lower, a low level is output. The PD pin goes to the high impedance state when the frequencies match.	
AIN AOUT	19 20	17 18	LPF amplifier transistors	The n-channel MOS transistor used for the PLL active low-pass filter.	
IFIN	12	11	IF counter	Accepts an input in the frequency range 0.4 to 12MHz. The input signal is directly transmitted to the IF counter. The result is output starting the MSB of the IF counter using the DO pin. Four measurement periods are supported: 4, 8, 32, and 64ms.	

DI Control Data (Serial Data Input) Structure

[1] IN1 mode



[2] IN2 mode



Control Data Functions

<table>
<tr><th>No.</th><th>Control block/data</th><th>Functions</th><th>Related data</th></tr>
<tr><td>(1)</td><td>Programmable divider data
P0 to P15</td><td>Data that sets the divisor of the programmable divider.
A binary value in which P15 is the MSB. The LSB changes depending on DVS and SNS. (*: don't care)
<table>
<tr><th>DVS</th><th>SNS</th><th>LSB</th><th>Divisor setting (N)</th><th>Actual divisor</th></tr>
<tr><td>1</td><td>*</td><td>P0</td><td>272 to 65535</td><td>Twice the value of the setting</td></tr>
<tr><td>0</td><td>1</td><td>P0</td><td>272 to 65535</td><td>The value of the setting</td></tr>
<tr><td>0</td><td>0</td><td>P4</td><td>4 to 4095</td><td>The value of the setting</td></tr>
</table>
Note: P0 to P3 are ignored when P4 is the LSB.

Selects the signal input pin (AMIN or FMIN) for the programmable divider, switches the input frequency range. (*: don't care)
<table>
<tr><th>DVS</th><th>SNS</th><th>Input pin</th><th>Input frequency range</th></tr>
<tr><td>1</td><td>*</td><td>FMIN</td><td>10 to 160MHz</td></tr>
<tr><td>0</td><td>1</td><td>AMIN</td><td>2 to 40MHz</td></tr>
<tr><td>0</td><td>0</td><td>AMIN</td><td>0.5 to 10MHz</td></tr>
</table>
Note: See the "Programmable Divider Structure" item for more information.</td><td></td></tr>
<tr><td>(2)</td><td>Reference divider data
R0 to R3</td><td>Reference frequency (fref) selection data.
<table>
<tr><th>R3</th><th>R2</th><th>R1</th><th>R0</th><th>Reference frequency</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>100kHz</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>50</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>25</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>25</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>12.5</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>6.25</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>3.125</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>3.125</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>10</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>9</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>5</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>3</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>15</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>* PLL INHIBIT + X'tal OSC STOP</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>* PLL INHIBIT</td></tr>
</table>
Note *: PLL INHIBIT
The programmable divider block and the IF counter block are stopped, the FMIN, AMIN, and IFIN pins are set to the pull-down state (ground), and the charge pump goes to the high impedance state.

Crystal resonator selection
XS=0: 4.5MHz
XS=1: 7.2MHz
The 7.2MHz frequency is selected after the power-on reset.</td><td></td></tr>
<tr><td>(3)</td><td>IF counter control data
CTE
GT0, GT1</td><td>IF counter measurement start data
CTE=1: Counter start
=0: Counter reset
Determines the IF counter measurement period.
<table>
<tr><th>GT1</th><th>GT0</th><th>Measurement time (ms)</th><th>Wait time (ms)</th></tr>
<tr><td>0</td><td>0</td><td>4</td><td>3 to 4</td></tr>
<tr><td>0</td><td>1</td><td>8</td><td>3 to 4</td></tr>
<tr><td>1</td><td>0</td><td>32</td><td>7 to 8</td></tr>
<tr><td>1</td><td>1</td><td>64</td><td>7 to 8</td></tr>
</table>
Note: See the "IF Counter Structure" item for more information.</td><td>IFS</td></tr>
</table>

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<table>
<tr><th>No.</th><th>Control block/data</th><th>Functions</th><th>Related data</th></tr>
<tr><td>(4)</td><td>I/O port specification data
IOC1, IOC2</td><td>Specifies the I/O direction for the bidirectional pins $\overline{IO1}$ and $\overline{IO2}$.
Data: 0=input mode, 1=output mode</td><td></td></tr>
<tr><td>(5)</td><td>Output port data
BO1 to BO4
IO1, IO2</td><td>Data that determines the output from the $\overline{BO1}$ to $\overline{BO4}$, $\overline{IO1}$ and $\overline{IO2}$ output ports
Data: 0=open, 1=low
The data=0 (open) state is selected after the power-on reset.</td><td>IOC1
IOC2</td></tr>
<tr><td>(6)</td><td>DO pin control data
DOC0
DOC1
DOC2</td><td>Data that determines the DO pin output
<table>
<tr><th>DOC2</th><th>DOC1</th><th>DOC0</th><th>Do pin state</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Open</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Low when the unlock state is detected</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>end-UC *1</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Open</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Open</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>The $\overline{IO1}$ pin state *2</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>The $\overline{IO2}$ pin state *2</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Open</td></tr>
</table>
The open state is selected after the power-on reset.
Note: 1. end-UC: Check for IF counter measurement completion
(1) When end-UC is set and the IF counter is started (i.e., when CTE is changed from zero to one), the DO pin automatically goes to the open state.
(2) When the IF counter measurement completes, the DO pin goes low to indicate the measurement completion state.
(3) Depending on serial data I/O (CE: high) the DO pin goes to the open state.
Note: 2. Goes to the open state if the I/O pin is specified to be an output port.
Caution: The state of the DO pin during a data input period (an IN1 or IN2 mode period with CE high) will be open, regardless of the state of the DO control data (DOC0 to DOC2). Also, the DO pin during a data output period (an OUT mode period with CE high) will output the contents of the internal DO serial data in synchronization with the CL pin signal, regardless of the state of the DO control data (DOC0 to DOC2).</td><td>UL0, UL1
CTE

IOC1
IOC2</td></tr>
<tr><td>(7)</td><td>Unlock detection data
UL0, UL1</td><td>Selects the phase error (E) detection width for checking PLL lock.
A phase error in excess of the specified detection width is seen as an unlocked state.
Note: In the unlocked state the DO pin goes low and the UL bit in the serial data becomes zero.</td><td>DOC0
DOC1
DOC2</td></tr>
</table>

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Control Data Functions

No.	Control block/data	Functions	Related data
(1)	I/O port data I2, I1	Latched from the pin states of the $\overline{IO1}$ and $\overline{IO2}$ I/O ports. These values follow the pin states regardless of the input or output setting. I1 $\overline{IO1}$ pin state High: 1 I2 $\overline{IO2}$ pin state Low: 0	IOC1 IOC2
(2)	PLL unlock data UL	Latched from the state of the unlock detection circuit. UL 0: Unlocked UL 1: Locked or detection stopped mode	UL0 UL1
(3)	IF counter binary counter C19 to C0	Latched from the value of the IF counter (20-bit binary counter). C19 MSB of the binary counter C0 LSB of the binary counter	CTE GT0 GT1

Serial Data I/O Methods

The LC72131K/KMA inputs and outputs data using Our CCB (computer control bus) audio LSI serial bus format. This LSI adopts an 8-bit address format CCB.

	I/O mode	Address								Function
		B0	B1	B2	B3	A0	A1	A2	A3	
[1]	IN1 (82)	0	0	0	1	0	1	0	0	Control data input mode (serial data input) 24 data bits are input. See the “DI Control Data (serial data input) Structure” item for details on the meaning of the input data.
[2]	IN2 (92)	1	0	0	1	0	1	0	0	Control data input mode (serial data input) 24 data bits are input. See the “DI Control Data (serial data input) Structure” item for details on the meaning of the input data.
[3]	OUT (A2)	0	1	0	1	0	1	0	0	

Programmable Divider Structure

	DVS	SNS	Input pin	Set divisor	Actual divisor: N	Input frequency range
(A)	1	*	FMIN	272 to 65535	Twice the set value	10 to 160MHz
(B)	1	1	AMIN	272 to 65535	The set value	2 to 40MHz
(C)	0	0	AMIN	4 to 4095	The set value	0.5 to 10MHz

*: Don't care

Programmable Divider Calculation Examples

(1) FM, 50kHz steps (DVS=1, SNS=*: FMIN selected)
FM RF=90.0MHz (IF=+10.7MHz)
FM VCO=100.7MHz
PLL fref=25kHz (R0 to R1=1, R2 to R3=0)
100.7MHz (FMVCO) 25kHz (fref) 2 (FMIN: divide-by-two prescaler) =2014 07DE (HEX)

(2) SW 5kHz steps (DVS=0, SNS=1: AMIN high-speed side selected)
SW RF=21.75MHz (IF=+450kHz)
SW VCO=22.20MHz
PLL fref=5kHz (R0=R2=0, R1=R3=1)
22.2MHz (SW VCO) 5kHz (fref) =4440 1158 (HEX)

(3) MW 10kHz steps (DVS= DVS= se047l.2455o.0006 T-s7605 p.0006 1.4(0 -RF=7605 ( )Tj/)3.9(0.)5.4(0M)9.8(w[174 (I)-5.5(F

IF Counter Operation

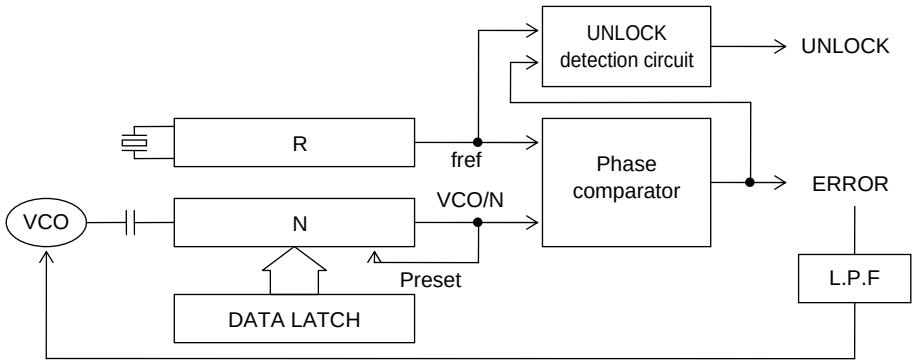

Figure 2 Circuit Structure

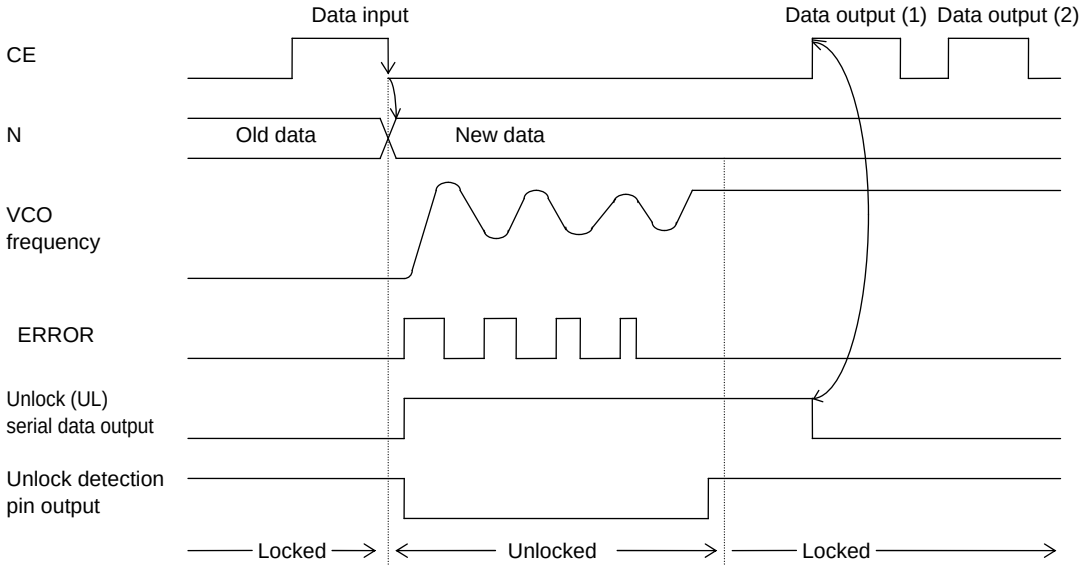

Figure 3

Unlocked State Data Output Using Serial Data Output

In the LC72131K/KMA, once an unlocked state occurs, the unlocked state serial data (UL) will not be reset until a data input (or output) operation is performed. At the data output (1) point in Figure 3, although the VCO frequency has stabilized (locked), since no data output has been performed since the divisor N was changed the unlocked state data remains in the unlocked state. As a result, even though the frequency has stabilized (locked), the system remains (from the standpoint of the data) in the unlocked state.

Therefore, the unlocked state data acquired at data output (1), which occurs immediately after the divisor N was changed, should be treated as a dummy data output and ignored. The second data output (data output (2)) and following outputs are valid data.

<Locked State Determination Flowchart Example>

Valid data can be output at

Directly Outputting Unlocked State Data from the DO Pin (Set by the DO pin control data)

Since the unlocked state (high=locked, low=unlocked) is output directly from the DO pin, the dummy data processing described in section 3 above is not required. After changing the divisor N, the locking state can be checked after waiting at least two reference frequency periods.

Clock Time Base Usage Notes

The pull-up resistor used on the clock time base output pin ($\overline{BO1}$) should be at least 100k . This is to prevent degrading the VCO C/N characteristics when a loop filter is

Dead Zone

Pin States After the Power ON Reset [LC72131KMA]

Application System Example

Application System Example [LC72131KMA]