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ORDERING INFORMATION

Continued from preceding page.

Parameter	Symbol	Conditions	Ratings min	Ratings typ	Ratings max	Unit
RDY width (corrected output read)	t_{WDRDY}	RDY (BUSWD=L 8bits)	60		210	nS
		RDY ((BUSWD=H 16bits)	300		490	nS
DACK to DREQ delay	t_{DREQ}	DREQ, DACK			260	nS
DMA cycle wait	t_{CYDM}	RD, DREQ			420	nS
RD low-level width (DMA)	t_{WRDM}	RD	300			nS

Notes: Application designs must take the RDY signal output delay into consideration if the RDY signal is used as the CPU bus wait signal.
If the RDY signal is not used, (that is, if no wait states are inserted) the value of the RD low-level width will be 250ns (minimum).

[LC72711LW]

Allowable Operating Ranges at Ta=-40 to +85°C, V_{SS}=0V

Parameter	Symbol	Conditions	Ratings min	Ratings typ	Ratings max	Unit
Supply voltage	V_{DD}		2.7		3.6	V
High-level input voltage	$V_{IH}1$	A0/CL, A1/CE, A2/DI, RST, STNBY	$0.7V_{DD}$		5.5	V
	$V_{IH}2$	DACK, WR, RD, CS, SP, BUSWD, A3, IOCNT1, IOCNT2	$0.7V_{DD}$		V_{DD}	V
Low-level input voltage	$V_{IL}1$	Pins for which $V_{IH}1$ applies	V_{SS}		$0.3V_{DD}$	V
	$V_{IL}2$	Pins for which $V_{IH}2$ applies	V_{SS}		$0.3V_{DD}$	V
Oscillator frequency	F_{OSC}	This IC operates with a frequency precision of ±250 ppm		7.2		MHz
XIN input sensitivity	V_{XI}	With a sine wave input to XIN, capacitor coupling, V_{DD}=+2.7 to +3.6V	400		900	mVrms
Input amplitude	$V_{MPX}1$	With a 100% modulated composite signal input to MPXIN, V_{DD}=+3.3V	120		350	mVrms
	$V_{MPX}2$	With a 100% modulated composite signal input to MPXIN, V_{DD}=+2.7V	120		180	mVrms
[Serial I/O]						
Clock low-level period	t_{CL}	A0/CL	0.7			µS
Clock high-level period	t_{CH}	A0/CL	0.7			µS
Data setup time	t_{SU}	A0/CL, A2/DI	0.7			µS
Data hold time	t_{HD}	A0/CL, A2/DI	0.7			µS
CE wait time	t_{EL}	A0/CL, A1/CE	0.7			µS
CE setup time	t_{ES}	A0/CL, A1/CE	0.7			µS
CE hold time	t_{EH}	A0/CL, A1/CE	0.7			µS
Data latch change time	t_{LC}	A1/CE			0.7	µS
Data output time	t_{DDO}	DO, A0/CL	277		555	nS
CRC4 change time	t_{CRC}	CRC4, A0/CL			0.7	µS

[LC72711LW]

Allowable Operating Ranges: Parallel Interface at Ta=-40 to +85°C, V_{SS}=0V

Parameter	Ratings

Continued from preceding page.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
DMA cycle wait	t_{CYDM}	RD, DREQ			420	nS
RD low-level width (DMA)	t_{WRDM}	RD	300			nS

Notes: Application designs must take the RDY signal output delay into consideration if the RDY signal is used as the CPU bus wait signal.
If the RDY signal is not used, (that is, if no wait states are inserted) the value of the RD low-level width will be 280ns (minimum).

[LC72711W]

Electrical Characteristics at V_{DD}=+4.5 to +5.5V, within the allowable operating ranges

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
High-level output voltage	$V_{OH}1$	I_O=2mA, BCK, FCK, BLOCK, FLOCK, CRC4, CLK16, DATA	V_{DD}-0.4			V
	$V_{OH}2$	I_O=4mA, INT, RDY, DREQ, D0 to D15	V_{DD}-0.4			V
Low-level output voltage	$V_{OL}1$	I_O=2mA, Pins for which $V_{OH}1$ applies			0.4	V
	$V_{OL}2$	I_O=4mA, Pins for which $V_{OH}2$ applies			0.4	V
	$V_{OL}3$	I_O=2mA, DO, INT			0.4	V
High-level input current	$I_{IH}1$	V_{IN}=5.5V, A0/CL, A1/CE, A2/DI, RST, STNBY			1.0	µA
	$I_{IH}2$	V_{IN}=V_{DD}D, All input pins other than $I_{IH}1$			1.0	µA
Low-level input current	I_{IL}	V_{IN}=V_{SS}D, All input pins			-1.0	µA
Input resistance	R_{MPX}	MPXIN -Vssa f=100kHz		50		kΩ
Reference supply voltage output	Vref	Vref, Vdda=5V		2.5		V
Bandpass filter center frequency	Fc	FLOUT		76.0		kHz
-3 dB bandwidth	Fbw	FLOUT		19.0		kHz
Group delay	Dgd	FLOUT	-7.5		+7.5	µs
Gain	Gain	FLOUT-MPXIN, f=76kHz		20		dB
Stop band attenuation	ATT1	FLOUT, f=50kHz	25			dB
	ATT2	FLOUT, f=100kHz	15			dB
	ATT3	FLOUT, f=30kHz	50			dB
	ATT4	FLOUT, f=150kHz	50			dB
Output off leakage current	I_{OFF}	VO=V_{DD}D, DO			5.0	µA
Hysteresis voltage	V_{HYS}	A0/CL, A1/CE, A2/DI, A3, CS, RD, WR, DACK, IOCNT1, IOCNT2, RST, STNBY		0.1V_{DD}D		V
Internal feedback resistor	Rf	XIN, XOUT		1.0		MΩ
Current drain	I_{DD}			18	25	mA

[LC72711LW]

Electrical Characteristics at V_{DD}=+2.7 to +3.6V, within the allowable operating ranges

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
High-level output voltage	$V_{OH}1$	I_O=1mA, BCK, FCK, BLOCK, FLOCK, CRC4, CLK16, DATA	V_{DD}-0.4			V
	$V_{OH}2$	I_O=2mA, INT, RDY, DREQ, D0 to D15	V_{DD}-0.4			V
Low-level output voltage	$V_{OL}1$	I_O=1mA, Pins for which $V_{OH}1$ applies			0.4	V
	$V_{OL}2$	I_O=2mA, Pins for which $V_{OH}2$ applies			0.4	V
	$V_{OL}3$	I_O=1mA, DO, INT			0.4	V
High-level input current	$I_{IH}1$	V_{IN}=5.5V, A0/CL, A1/CE, A2/DI, RST, STNBY			1.0	µA
	$I_{IH}2$	V_{IN}=V_{DD}D, All input pins other than $I_{IH}1$			1.0	µA
Low-level input current	I_{IL}	V_{IN}=V_{SS}D, All input pins			-1.0	µA
Input resistance	R_{MPX}	MPXIN -Vssa f=100kHz		50		kΩ
Reference supply voltage output	Vref	Vref, Vdda=3V		1.5		V
Bandpass filter center frequency	Fc	FLOUT		76.0		kHz
-3 dB bandwidth	Fbw	FLOUT		19.0		kHz
Group delay	Dgd	FLOUT	-7.5		+7.5	µs
Gain	Gain	FLOUT-MPXIN, f=76kHz		20		dB
Stop band attenuation	ATT1	FLOUT, f=50kHz	25			dB
	ATT2	FLOUT, f=100kHz	15			dB
	ATT3	FLOUT, f=30kHz	50			dB
	ATT4	FLOUT, f=150kHz	50			dB
Output off leakage current	I_{OFF}	VO=V_{DD}D, DO			1.0	µA

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Parameter	Symbol	Conditions	Ratings min	Ratings typ	Ratings max	Unit
Hysteresis voltage	V_{HYS}					

Continued from preceding page.

Pin No.	Pin	Function	I/O	Pin circuit
17 to 24	D0 to D7	Data bus The bus width can be set to be either 8 bits or 16bits by the BUSWD		

Continued from preceding page.

Address	Register	Function	R/W	Address	Register	Function	R/W
1	BIC	Number of allowable BIC errors	W	1	STAT	Status register	R
2	SYNCB	Block synchronization: error protection count	W	2	BLNO	Block number register	R
3	SYNCF	Frame synchronization: error protection count	W				
4	CTL1	Control register 1	W				
5	CTL2	Control register 2	W				
6	CRC4	Layer 4 CRC register	W				

Number of Allowable BIC Errors

Address	Register	R/W	Initial value	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
01H	BIC	W	22H	Back protection			(LSB)	Forward protection			(LSB)

The synchronization circuit in this IC operates by recognizing a 16-bit BIC code. The number of allowable errors is the number of incorrect bits allowed in those 16 bits. This data sets up separate values for forward protection mode (when synchronized) and for back protection mode (when not synchronized).
The default value is to allow 2 incorrect bits in both forward and back modes. If the block synchronization discrimination output (BLOCK) is used for discriminating whether or not FM multiplex data is present, we recommend setting the back protection mode BIC allowable error count to 1 or 0.

Block Synchronization: Error Protection Count

Address	Register	R/W	Initial value	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
02H	SYNCB	W	17H	Back protection			(LSB)	Forward protection			(LSB)

The synchronization protection count can be set separately for both forward and back protection. The count conditions for the protection counts are as follows.

- Back protection mode (not synchronized: BLOCK=low)
  If the timing of the IC internal synchronization free-running counter matches the timing of the received BIC, the protection count is incremented by 1. Contrarily, if the timings of the IC internal counter and the received BIC do not match, the protection counter is cleared to 0. The timing of the count is the timing of the IC internal counter.
- Forward protection mode (synchronized: BLOCK=high)
  In reverse to the back protection mode, if the timing of the IC internal free-running counter does not match the detection timing of the received BIC, the protection counter is incremented, and if the timings match, the protection counter is cleared to 0.

Figure 1 shows the states of the protection counter for the cases where the forward and back protection counts are both 3. This IC defines the value of the protection counter to be 1 at the point that a match or a discrepancy occures between the IC internal timing and the timing of the received BIC occurs. For example, when the value of the back protection count is 2, the IC internal timing and the timing of the received BIC will have matched two times consecutively.
If the protection data is set to new values, for example if the protection counts are set to 3 as assumed in figure 1, applications must send values which are 1 less than the intended value; in this case 22H. Similarly, if the value is set to 00H, the protection counts will, by definition, be set to 1 for both the forward and back directions. However, note that the resulting operation will be equivalent to there being no protection circuit. The default values are 8 for the forward protection count and 2 for the back protection count.
If the block synchronization output (BLOCK) is used for discriminating whether or not FM multiplex data is present, we recommend setting the block synchronization back protection count to a value that is more strict than the default value. (That is, we recommend replacing the default value of 2 with a value of 3 or higher.)

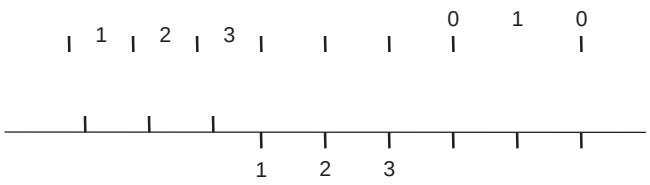


Figure 1 Block Synchronization Protection Operation (Forward → Back → Forward)

Frame Synchronization: Error Protection Count

Address	Register	R/W	Initial value	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
03H	SYNCF	W	17H	Back protection			(LSB)	Forward protection			(LSB)

This IC detects the BIC characteristic inflection points which occur at four places in a single frame, and increments or decrements a protection counter depending on whether or not they match the IC internal frame synchronization timing counter.
As is the case with the block synchronization error protection value, applications must set these to values one less than the desired protection count. The default values are 8 for the frame synchronization forward protection count and 2 for the back protection count.

Control Register 1

Address	Register	R/W	Initial value	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
04H	CTL1	W	00H	CRC4_RST	DO_MOVE	INT_MOVE	SYNC_RST	EC_STOP	VEC_HALT	RTIB	FRAME

・FRAME
0: Specifies method B. (default)
1: Specifies method A.

・RTIB
0: Real-time information blocks present. (default)
1: No real-time information blocks.
In the ITU-R recommended frame structure method A, a total of 12 data blocks can be inserted in the parity data area (the area that consists of 82 consecutive blocks of parity packets). If this IC is used in a system that has no real-time information blocks (RTIB), this flag must be set.
Note that if this flag is changed, frame synchronization is retained in the synchronized state for the time corresponding to the forward protection count, and then switches to the unsynchronized state. To quickly reestablish frame synchronization, applications must reset the synchronization circuit using the SYNC_RST flag.

・VEC_HALT
0: Vertical correction and the second horizontal correction processing are performed. (default)
1: Vertical correction and the second horizontal correction processing are not performed.
All IC operations related to vertical correction and the second horizontal correction are stopped by setting this flag.
Note that in data output, only data to which the first horizontal correction has been applied will be output.

・EC_STOP
0: All functions operate. (default)
1: Only the MSK detection circuit and the synchronization regeneration circuit operate.
This flag stops all operations relating to error correction (including RAM access), data output, and other operations. While all IC operations are stopped in standby mode, MSK demodulation, the synchronization circuit, the serial data input circuit, and the layer 4 CRC circuit continue to operate in this mode.

・SYNC_RST
0: (default)
1: Resets just the synchronization regeneration circuit.
Clears the synchronization status and the synchronization protection status in the synchronization circuit block, and sets the circuit to the unsynchronized state. This allows the circuit to quickly pull in to frame synchronization when the frame synchronization is incorrect for the new reception data following tuning, when the radio has been tuned to a new station. While this flag is used for synchronization related sections of the system, it does not initialize the registers that set the number of allowable BIC errors, the block synchronization forward and back protection counts, and the frame synchronization forward and back protection counts. Also note that during a synchronization block reset, the INT signal is not output and the DO pin outputs a high level (high-impedance).
This flag is not automatically reset to 0. Applications must send a 0 value after setting this flag.

・INT_MOVE
0: Data is only output when error correction has completed, layer 2 CRC has completed, and the data was received with the circuit synchronized. (default)
1: All data is output. (Operation is identical to that of the LC72700E.)
In the default state, this IC only outputs data that has been fully error corrected and that was received in both block and frame synchronization. (This also includes the layer 2 CRC check.)
To acquire all data as provided by the LC72700, applications must set both this flag and the VEC_OUT (BIT2) flag in control register 2 as described below.

.

Layer 4 CRC Register

Address	Register	R/W	Initial value	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
06H	CRC4	W	00H								(LSB)

This is the data group write register used for the layer 4 CRC check. It is used only when the parallel interface is used. Applications should specify the dedicated CCB address when using the serial interface.

Status Register

Address	Register	R/W	Initial value	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
01H	STAT	R	-	VH	BLK	FRM	ERR	PRI	HEAD	CRC4	RTIB

・VH
0: Indicates data for which only horizontal correction was performed.
1: Indicates data for which after horizontal correction, vertical and then second horizontal correction were performed as well.
Packet data with an RTIB flag is output with VH set to 0.

・BLK
0: Indicates data that was received with block synchronization unsynchronized.
1: Indicates data that was received with block synchronization synchronized.

・FRM
0: Indicates data that was received with frame synchronization unsynchronized.
1: Indicates data that was received with frame synchronization synchronized.

・ERR
0: Indicates data for which error correction completed and no errors were detected in the level 2 CRC check.
1: Indicates data for which error correction was not possible or for which errors were detected in the level 2 CRC check.

・PRI
0: Indicates data that was inferred to be data block data by the frame synchronization circuit.
1: Indicates data that was inferred to be parity block data by the frame synchronization circuit.
Packet data with an RTIB flag is output with PRI set to 0.

・HEAD
0:
1: Indicates data that was inferred to be in the frame head block by the frame synchronization circuit.
This flag is valid only when VH is 0.

・CRC4
0: Indicates that the layer 4 CRC detection circuit division registers were not all zeros.
1: Indicates that the layer 4 CRC detection circuit division registers were all zeros, i.e. that there were no errors.
The result at the point immediately prior to register readout is loaded into this flag.

・RTIB
0:
1: Indicates the data is a real-time information block. (This bit is valid only in method A'.)
This bit is fixed at 0 during method A and method B reception.

Data Update Timing for Read Registers

The data in the two read registers (the status register at address 01H and the block number register at address 02H) is updated in the 1 ms interval between 1 ms prior to the output of the interrupt control signal (INT) and a point immediately before the INT output.

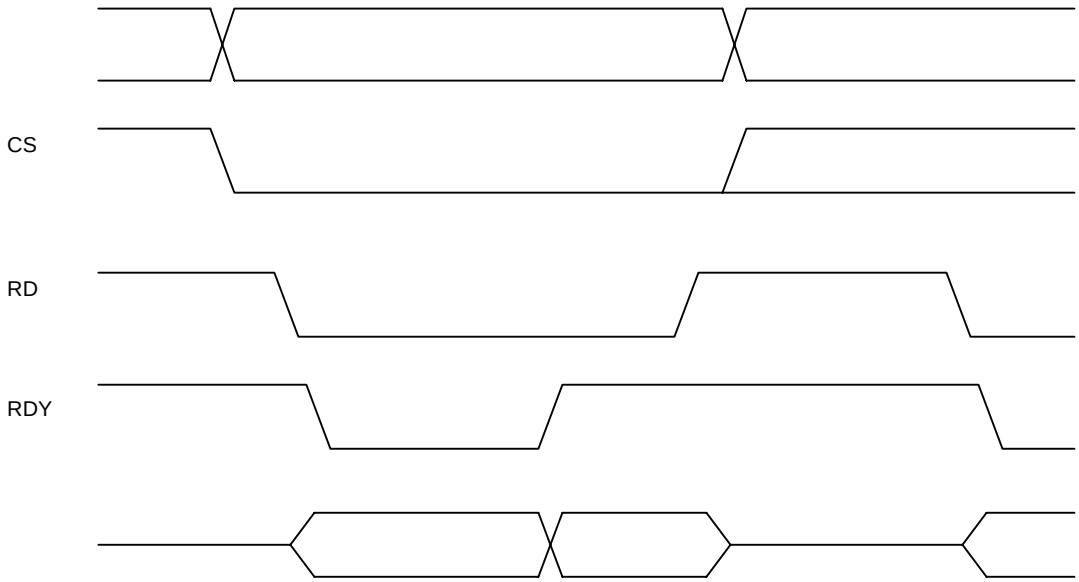
In normal processing, when an interrupt occurs, the application will first determine the nature of the data packet that will be output by the current interrupt signal by reading out the status register, and determine if it is necessary to read out that data. For example, if error correction failed and the erroneous data is not required, the application should simply wait for the next interrupt.

If the CCB interface is used, the application reads out the data from CCB address #FB, and determines the status from the additional 16 bits of data. It then either reads out the following data or sets the CE signal low to cancel the readout.

Applications can also read out data asynchronously with respect to the interrupt signal. In this case, the application checks the current reception status by reading out the status register and checking bit 6 (data received in the block synchronized state) and bit 5 (data received in the frame synchronized state). In this case, using data for which bit 7 (VH) is 0 provides superior real time characteristics.

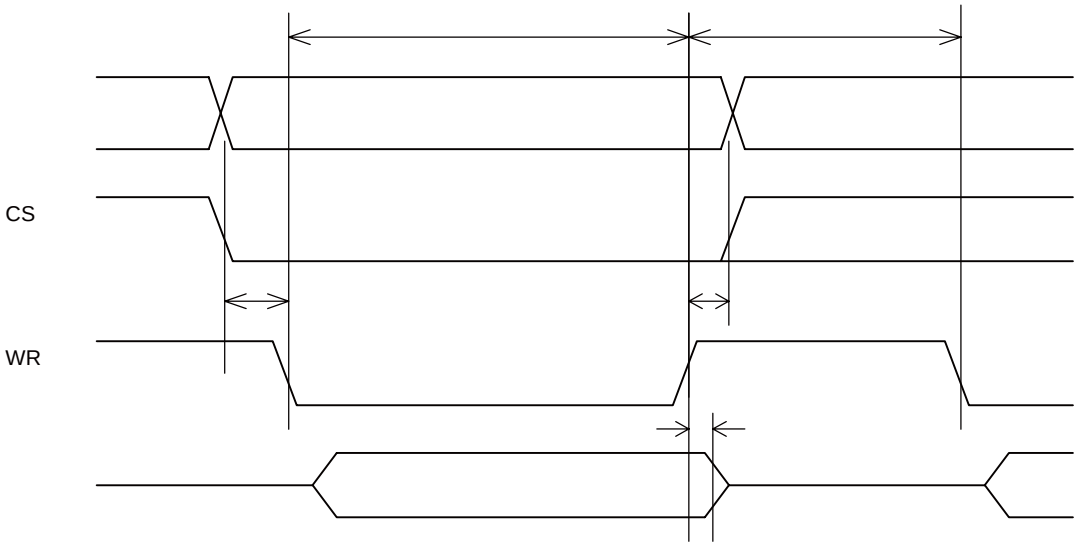
CPU Interface Timing <Parallel Mode>

・Register Read Timing

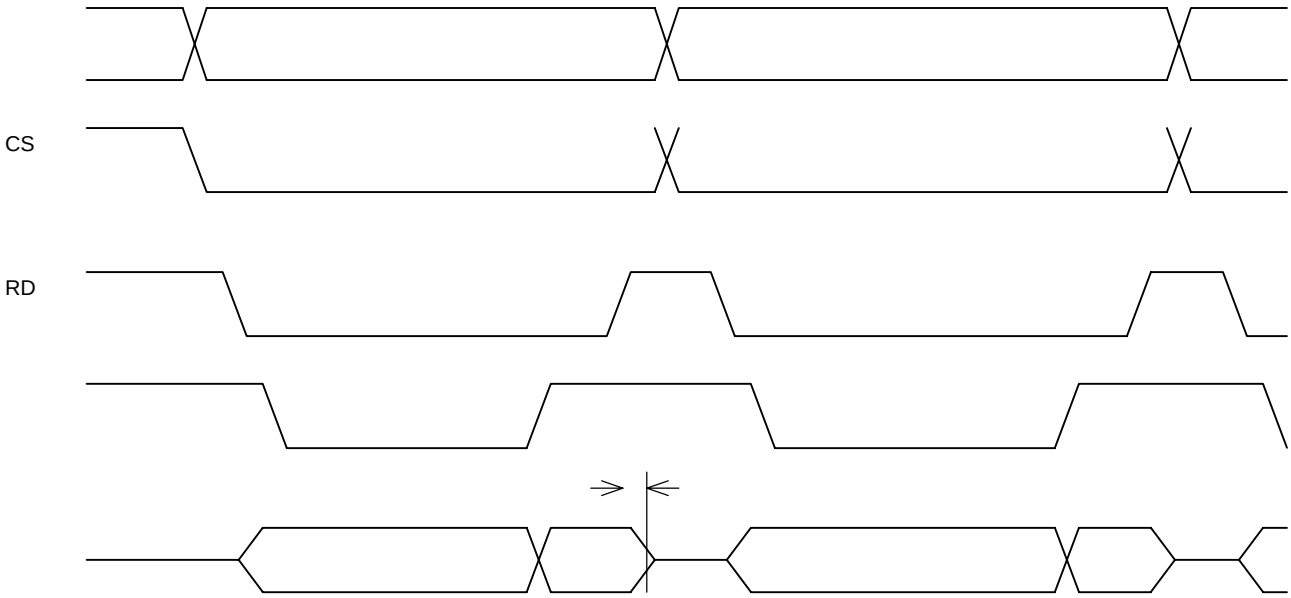


* t_{HARD} stipulates the earliest timing for A0 to A3 and CS.

・Register Write Timing



・Post-Correction Data Read Timing



・Post-Correction Data Read Timing (DMA)

Layer 4 CRC Detection Circuit <Parallel Interface>

This function provides data group error detection, i.e. layer 4 CRC. When the stipulated number of bytes of data group data and the CRC detection word (16 bits) are written to the layer 4 CRC register (address 6), if either the CRC4 pin outputs a high level or the CRC4 flag (bit 1 in the status register at address 1) is set to 1 then there were no errors in the data. The CRC4 pin or CRC4 flag in the status register outputs a high level if the IC internal CRC detection register bits are all in the logic 0 state.

When this function is used to perform a layer 4 CRC check, applications must initialize the IC internal CRC detection register before transferring the data for a single data group. This initialization is performed by sending data for bit 7 (CRC4_RST) in control register 1. Note that since this initialization flag is not automatically reset to 0, after the application sets this flag it must then send another data item that resets it to 0 before sending the layer 4 CRC check data.

If there were no errors in all the received data groups, the CRC register will, necessarily, be all zeros after the CRC check for a given data group. Therefore, as long as there are no errors detected in the layer 4 CRC check, the application does not need to initialize the CRC detection register again using the control register as described above. There is no upper limit on the total data length of data groups that can be transferred. Also, when the serial interface issued, the CCB transfers can be divided into multiple transfer operations. The generating polynomial G(x) for the CRC code is as follows. $G(x) = X^{16} + X^{12} + X^5 + 1$

Structure of the Post-Correction Output Data <Parallel Interface>

The total length of the prepared output data is always 176 bits, i.e. 22 bytes. The layer 2 CRC data (14 bits) and the parity data (82 bits) are not output. The data in each packet in the post-correction data is output in order starting at the beginning in 8- or 16-bit units. BIC codes are not output.

When the CPU reads out the data, it can easily select the data by checking the status register first. The CPU can then simply ignore data determined to be unnecessary without having to read it out by simply waiting until the next interrupt arrives.

CPU Interface <CCB Mode>

CCB Format

Data is input and output using the CCB (Computer Control Bus) format, which is ON Semiconductor's audio IC serial bus format. This IC uses an 8-bit address CCB with the address shown below. The CCB address is sent while CE is low, and the CCB I/O mode is determined when CE is set high.

I/O mode	CCB address								Item
	B0	B1	B2	B3	A0	A1	A2	A3	
Input	0	1	0	1	1	1	1	1	16-bit control data input
Output	1	1	0	1	1	1	1	1	Data corresponding to the number of clock (CL) cycles is output
Input	0	0	1	1	1	1	1	1	Data input mode for the layer 4 CRC detection circuit (8-bit units)
Output	1	0	1	1	1	1	1	1	Register output only

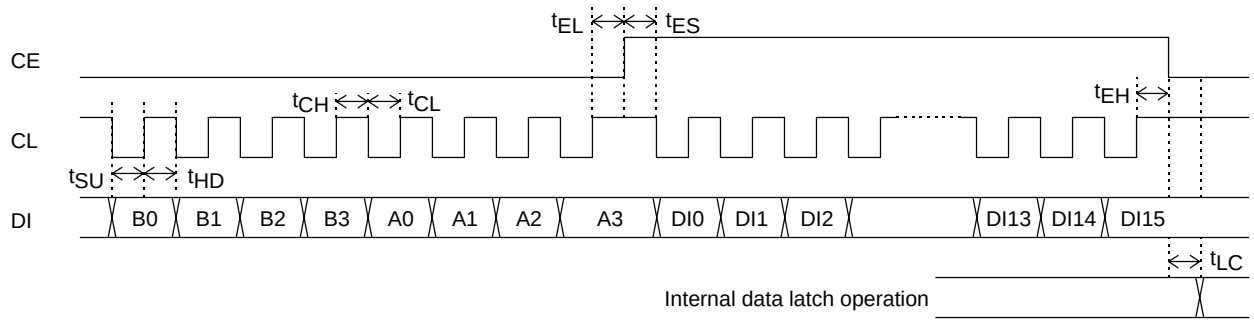
Data input (Register write)

Data is stored in an IC internal register. The CCB address #FA and 16 bits of data (DI0 to DI15) are input to the DI pin. The bits are assigned as follows. Although DI12 to DI15 are unused data, arbitrary values must be provided to complete a full 16 bits of data.

See the "Control Register" section earlier in this document for details on the register contents and addresses.

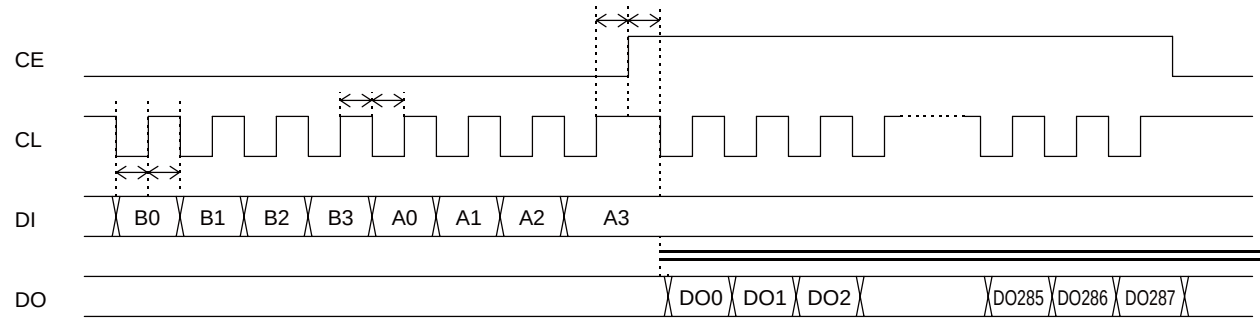
Details on writing to the layer 4 CRC check register are described later in this document. (The CCB address #FC is used for this function.)

DI0	DI1	DI2	DI3	DI4	DI5	DI6	DI7	DI8	DI9	DI10	DI11	DI12 to DI15
BIT0	BIT1	BIT2	BIT3	BIT4	BIT5	BIT6	BIT7	BIT0	BIT1	BIT2	BIT3	Unused data
(LSB)	Input data (8 bits)						(MSB)	Register address				



Data Output (Post-correction data output)

The IC outputs packet data to which error correction processing has be applied. The application inputs the CCB address #FB to DI.



*: The DO pin is normally left open.
Since the DO pin is an n-channel open-drain output, the data change time from a low-level output to a high-level output differs due to the pull-up resistor.

Structure of the Post-Correction Output Data <CCB Interface>

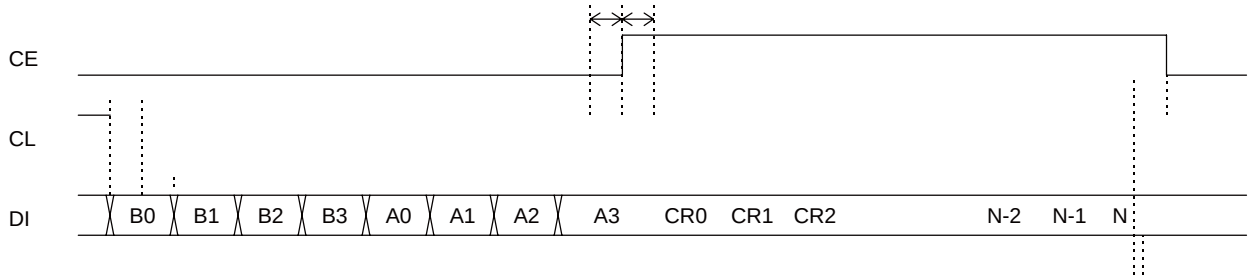
Post-error correction data can be output by using CCB address #FB. Although there are up to 288 bits of valid data that can be output, it is possible to stop clock input (CL input) and set CE to the low level, and output the remaining data on the next interrupt with no harmful effects whatsoever.

- The maximum amount of data that can be output is 288 bits (36 bytes), and the contents of the status register (STAT) and the block number register (BLNO) are added as the first two bytes.
- The contents of the STAT and BLNO registers are output LSB first.
- The post-correction data is output in order starting with the first bit in each single block of data.
- The BIC code is not output.
- The values of the output data are not guaranteed if multiple data read operations are performed for a single interrupt signal (INT).

STAT (8 bits)	BLNO (8 bits)	Data section (176 bits) Post-error correction data	Layer 2 CRC (14 bits)	Parity (82 bits)
DO0 to DO7	DO8 to DO15	DO16 to DO191	DO192 to DO205	DO206 to DO287

Layer 4 CRC Check Circuit <CCB Interface>

The basic outline of this operation is the same as that described in the Layer 4 CRC Detection Circuit <Parallel Interface> section earlier in this document. The data group data used for this error detection operation is sent to the IC using the CCB interface. The value #FC is used as the CCB address.
The data group data is transferred in 8-bit units. There is no upper limit on the amount of data that can be transferred (the value N in the figure below), and the data transfer may be divided into multiple operations.



Register Output

The IC internal status and block number registers are special-purpose registers that can be read out by applications. (See the discussion of the read register data update timing on page 12.)
The application inputs the CCB address #FD to DI. The status register data is output first followed by the block number register data.

Continued from preceding page.

This means that data that was fully corrected by horizontal correction is not output. Also, packet data that could not be corrected by either horizontal correction or vertical correction is not output. Furthermore, post-vertical correction parity packet data is also not output.

(4) Applications can clear the INT signal selection conditions described in (2) and (3) above by setting bit 5 (INT_MOVE) in the control register.

(5) Vertical correction is performed when all of the packet data in a frame is received in frame synchronization and furthermore when it was not possible to correct all of the packet (block) data with horizontal correction.
Vertical correction is not performed if one frame of data with no errors was received or the receiver was not in frame synchronization during reception.
To prevent incorrect correction, error correction using vertical correction is not performed for packets error correction using horizontal correction fully completed and for packets that had no errors.

(6) Under the default settings, if vertical correction is not performed, the corresponding post-vertical correction output is not output.
Applications can specify the post-vertical correction data to be output regardless of whether or not vertical correction is performed by setting bit 2 (VEC_OUT) in control register 2.

Note 1. In this case, if data with absolutely no errors is received, completely identical data will be output twice, once as horizontal correction output, and once as vertical correction output. This status is identical to the output status of the LC72700E.

Note 2. Immediately after power is applied, undefined data that is, in principle, not required by applications, will be output as post-vertical correction data.

CPU Interface Basic Limitations

Notes on Data Output Timing (Relationship with the received data)

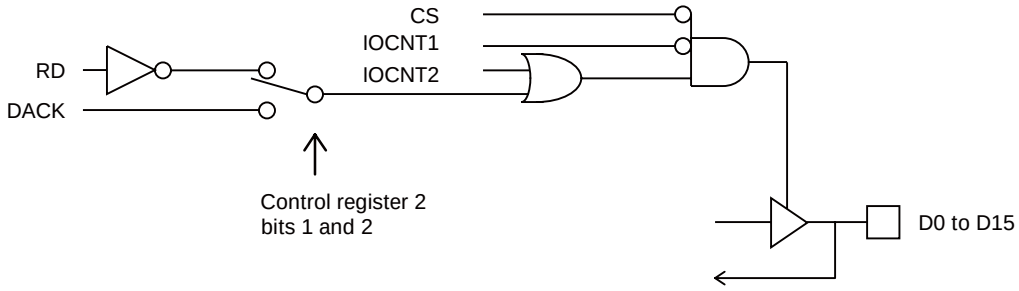
Figure 3 shows the timing relationship between the received data and the interrupt control signal (INT). However, the delay from the actual received signal due to demodulation operations in MSK demodulation blocks is ignored.
Block synchronization is established by discriminating the BIC code. As shown in figure 3, the data for the nth packet can be output during reception of the following packet (number n+1).
Figure 4 shows the output timing for post-vertical correction data. In vertical correction, the data for a single frame is stored in memory and the correction operation is performed if frame synchronization was established and it was not possible to correct all the packet data in horizontal correction. The timing with which vertical correction is started is the start of the frame. Horizontal correction is performed for each packet while packets 1 through 28 in the nth frame are being received, and this data is passed to the CPU interface. Vertical correction is performed for the data from the previous frame (frame n-1) in the unused time periods during that processing.
The vertical correction data consists of 190 blocks that are output, and this data is output at the rate of one block for every block

CPU Connection Example <Parallel Interface>

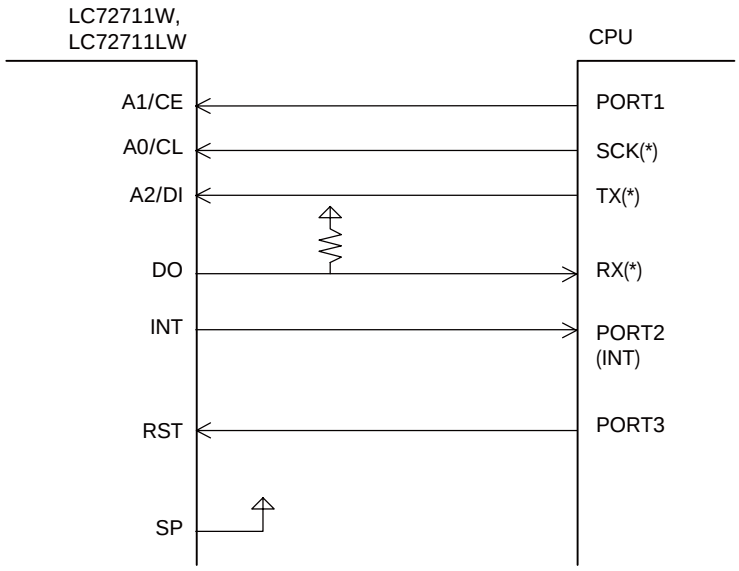
This section presents examples of the connection of this IC to a CPU.
Note that care is required with respect to read timing, since the time required to read a register, and the time required

・Data bus I/O control block

The data bus (D0 to D15) can be controlled with two control signals: IOCNT1 and IOCNT2.
These pins must be held low if unused.



CPU Connection example <CCB Interface>

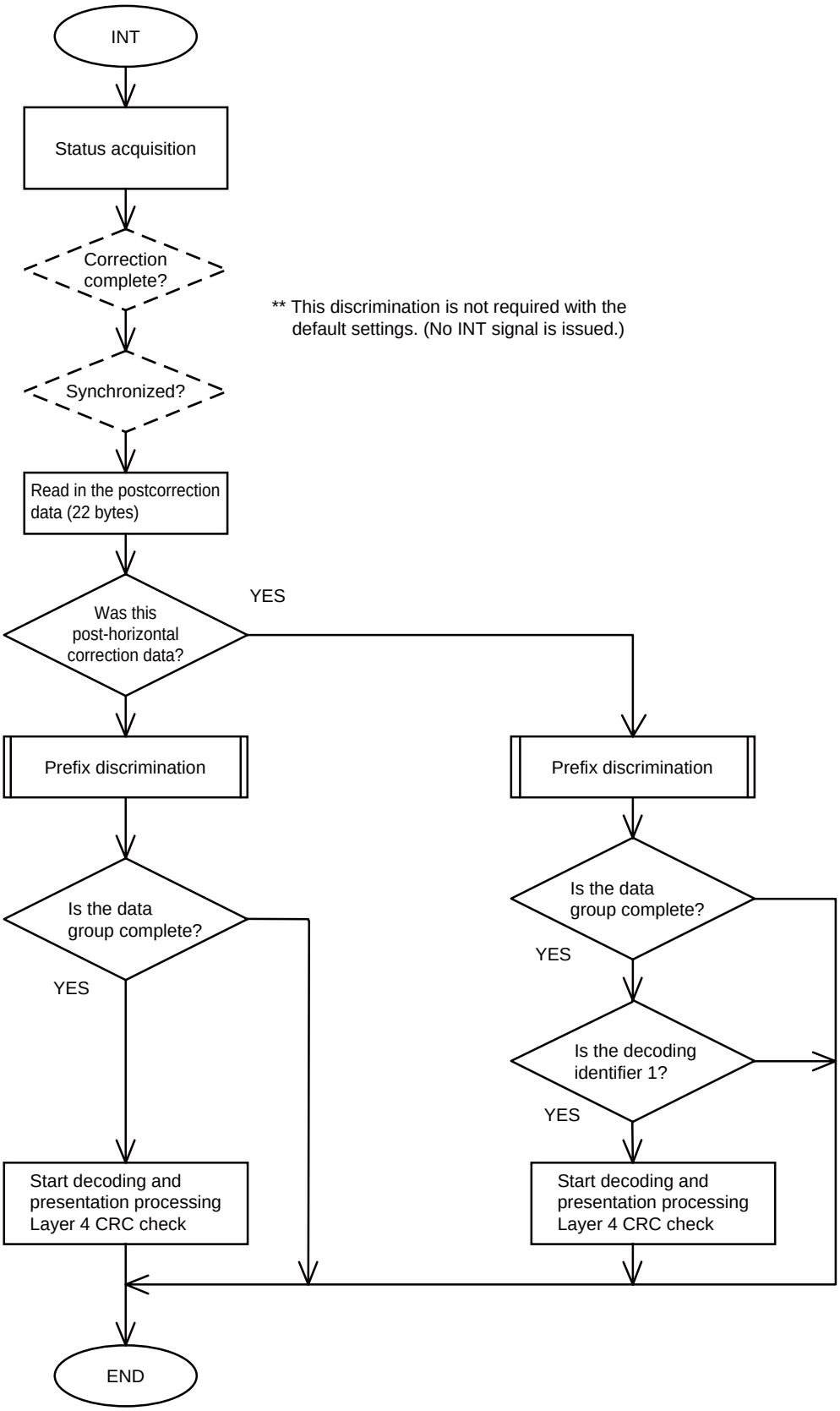


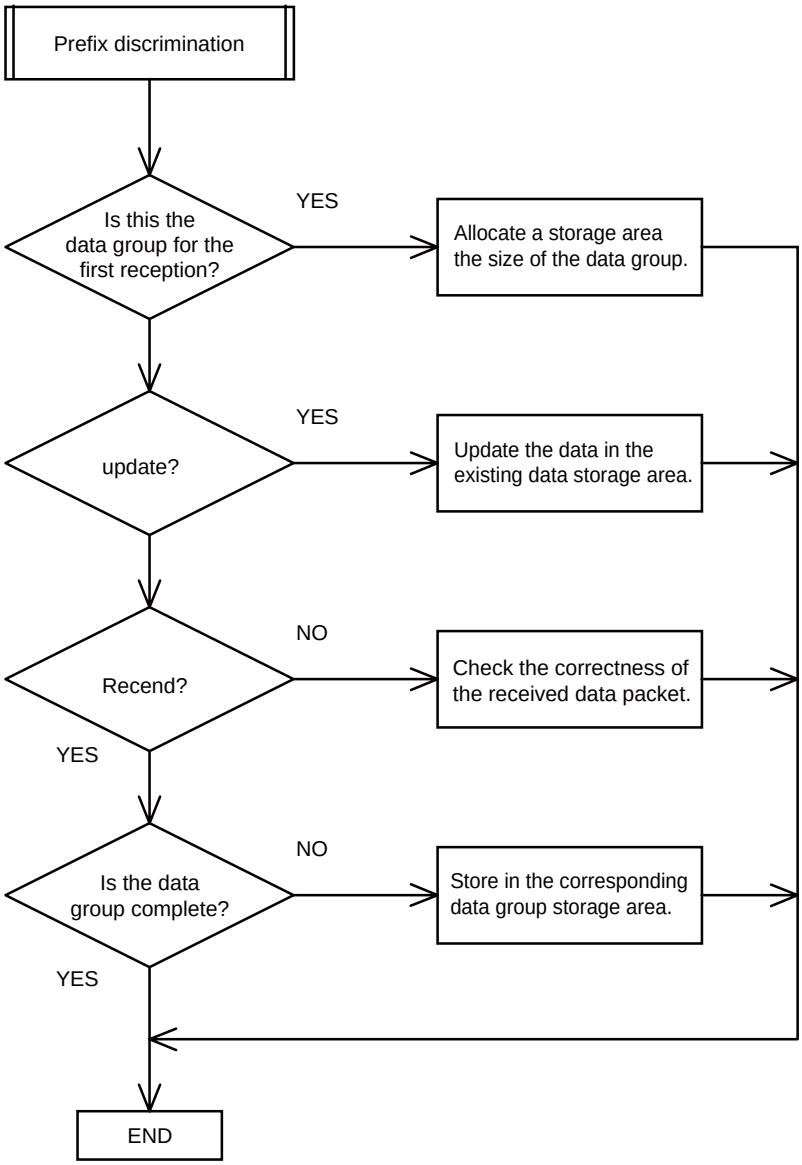
* SCK, TX, and RX are the CPU serial interface channel. Normally, I/O port pins may be used for these lines.
* The resistance of the DO pin pull-up resistor must be selected according to the transfer clock speed.

Control Program Compatibility

Sample Data Acquisition Flowchart

Note: The figure below is for allocation of received data at the layer 3 level.
This documentation is present as an example for reference purposes only of FM multiplex data acquisition processing by the system CPU. Its operation is not guaranteed.





Additional Notes

In addition to the above processing, processing required for layer 3 (data group) level processing includes “deletion of inappropriate data.” Although rare, in certain cases the IC will send inappropriate packet data that does not belong to any data group currently being broadcast. The following three points are possible reasons for this occurring.

(1) The IC frame synchronization circuit generates an incorrect synchronization state, and the IC incorrectly outputs parity packet data as normal packet data. This can occur when the back protection count is less rigorous (2 or lower), or during weak field reception.
(2) While extremely rare, incorrect correction can occur. (This almost never happens.)
(3) Noise entering the data transfer lines between the FMD IC and the CPU within the end product set.

Inappropriate packet data that occurs for these reasons and does not belong to any data group, will not be updated, and will remain in the program storage memory indefinitely. If the application does not include a routine that searches for and deletes inappropriate data, program storage memory will overflow at some point.

Also, applications should perform a layer 4 CRC check after data group completion and before program display.

Sample Application Circuit (CCB serial interface)