LC72717PW

Mobile FM Multiplex Broadcast (DARC) Receiver IC

ON Semiconductor®

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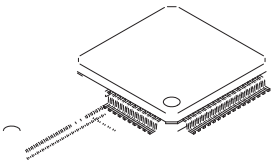

SPQFP64 10x10 / SQFP64

Overview

The LC72717PW is a data demodulation LSI for receiving FM multiplex broadcasts for mobile reception in the DARC format. This LSI includes an on-chip bandpass filter for extracting the DARC signal from the FM baseband signal. It also supports ITU-R recommended FM multiplex frame structures (methods A, A', B, and C) and can implement a compact, multifunction DARC reception system.

The LC72717PW's package, pin assignment and electrical characteristics are same as the LC72715PW (VICS-LSI). Functionally, the LC72717PW is a product that VICS function is removed from the LC72715PW.

The LC72717PW is also control-compatible with the LC72711LW.

Note that a contract with the NHK Engineering System, Inc. may be required to produce DARC compatible products in case, please contact with the NHK Engineering System, Inc.

Functions

Adjustment-free 76 kHz SCF bandpass filter
Supports all FM multiplex frame structures (methods A, A', B and C) under CPU control.
MSK delay detection system based on a 1T delay.
Error correction function based on a 2T delay (in the MSK detection stage)
Digital PLL based clock regeneration function
Shift-register 1T and 2T delay circuits
Block and frame synchronization detection circuits
Functions for setting the number of allowable BIC errors and the number of synchronization protection operations.
Error correction using (272, 190) codes
Built-in layer 4 CRC code checking circuit
On-chip frame memory and memory control circuit for vertical correction
7.2 MHz crystal oscillator circuit
Two power saving modes: STNBY and EC STOP
Applications can use either a parallel CPU interface (DMA) or a CCB* serial interface.
Supply voltage: 2.7 V to 3.6 V

* Computer Control Bus (CCB) is an ON Semiconductor's original bus format and the bus addresses are controlled by ON Semiconductor.

ORDERING INFORMATION

See detailed ordering and shipping information on page 27 of this data sheet.

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Publication Order Number :
LC72717PW/D

Specifications

Absolute Maximum Ratings at Ta = 25 C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD}		0.3 to +4.0	V
Input voltage	$V_{IN}1$	A0/CL, A1/CE, A2/DI, RST, STNBY (V_{DD} is equal to 2.7 V or more.)	0.3 to +5.6	V
		A0/CL, A1/CE, A2/DI, RST, STNBY (V_{DD} is less than 2.7 V.)	0.3 to V_{DD}+0.3	V
	$V_{IN}2$	Input pin other than $V_{IN}1$	0.3 to V_{DD}+0.3	V
Output voltage	V_{OUT}	Output pin	0.3 to V_{DD}+0.3	V
Output current	$I_{OUT}1$	INT, RDY, DREQ, D0 to D15, DO	0 to 2.0	mA
	$I_{OUT}2$	Output pin other than $I_{OUT}1$	0 to 1.0	mA
Allowable output current (total)	ITTL	Total for all the output pins	10	mA
Allowable power dissipation	Pd max		200	mW
Operating temperature	Topr	Ta 85 C	40 to +85	C
Storage temperature	Tstg		55 to +125	C

Allowable Operating Ranges at Ta = 40 C to +85 C, V_{SS} = 0 V

Parameter	Symbol	Pin Name	Type	Conditions	Ratings			unit
					min	typ	max	
Supply voltage	V_{DD}				2.7		3.6	V
Input high-level voltage	$V_{IH}1$	A0/CL, A1/CE, A2/DI, RST, STNBY	Schmitt		0.7V_{DD}		5.5	V
	$V_{IH}2$	IOCNT1, IOCNT2, DACK, D0, D1, D2, D3, D4, D5, D6, D7, WR, RD, A3, CS	Schmitt		0.7V_{DD}		V_{DD}	V
	$V_{IH}3$	SP, BUSWD, TIN, TPC1, TPC2, TOSEL1, TOSEL2			0.7V_{DD}		V_{DD}	V
Input low-level voltage	$V_{IL}1$	A0/CL, A1/CE, A2/DI, RST, STNBY	Schmitt		0.0		0.3V_{DD}	V
	$V_{IL}2$	IOCNT1, IOCNT2, DACK, D0, D1, D2, D3, D4, D5, D6, D7, WR, RD, A3, CS	Schmitt	120 500 mVrms	0.0		0.3V_{DD}	V
	$V_{IL}3$	SP, BUSWD, TIN, TPC1, TPC2, TOSEL1, TOSEL2			0.0		0.3V_{DD}	V
Oscillation frequency	FOSC	XIN, XOUT	Oscillation circuit	Within 250 ppm		7.2		MHz
XIN input sensitivity	VXI	XIN		Capacitive coupling	400			mVrms
Input amplitude	VMPX1	MPXIN	SCF	100% demodulation composite V_{DD} = 3.3 V	120		500	mVrms
	VMPX2	MPXIN	SCF	100% demodulation composite V_{DD} = 2.7 Vu Tc(V)Tjc				

Electrical Characteristics at Ta = 40 C to +85 C, V_{DD} = 2.7 V to 3.6 V, V_{SS} = 0 V

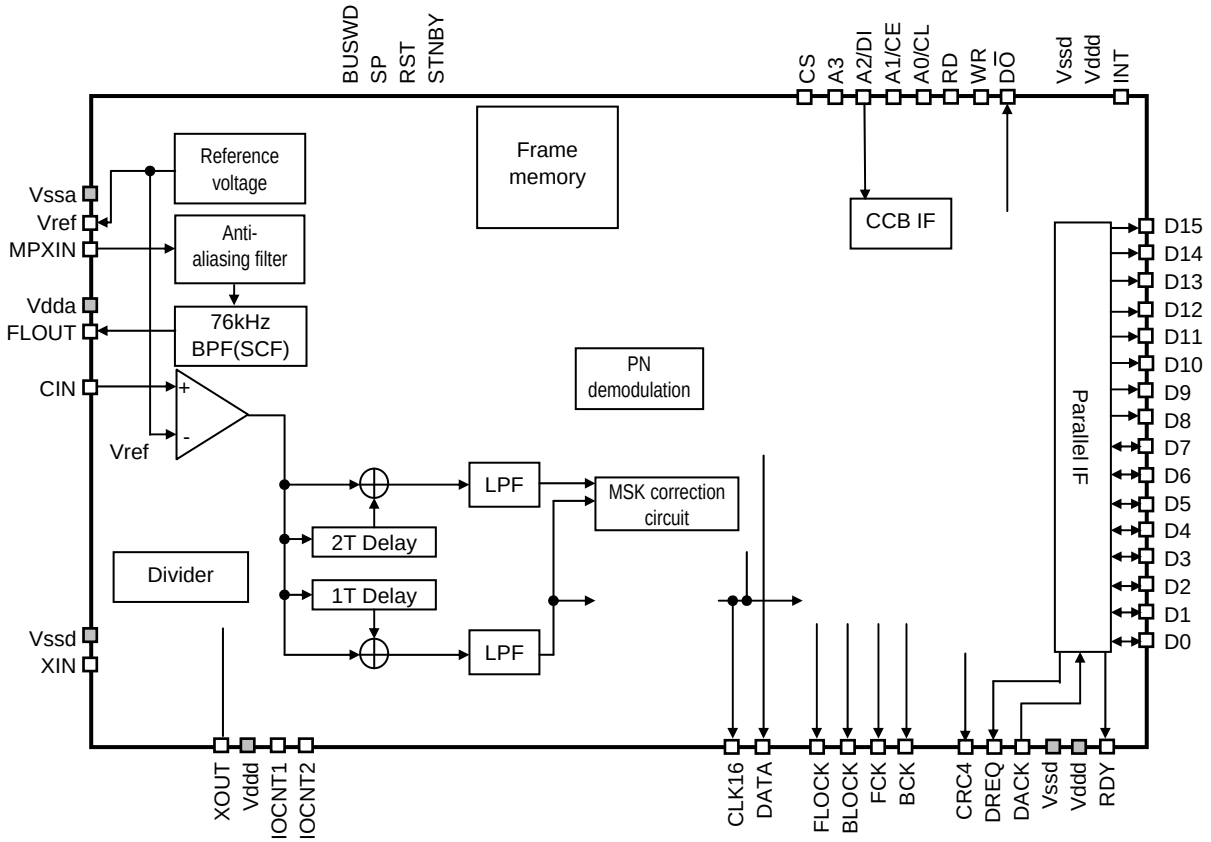
Parameter	Symbol	Pin Name	Type	Conditions	Ratings			unit
					min	typ	max	
Input high-level current	$I_{IH}1$	A0/CL, A1/CE, A2/DI, RST, STNBY	Schmitt				1.0	A
	$I_{IH}2$	IOCNT1, IOCNT2, DACK D0, D1, D2, D3, D4, D5, D6, D7, WR, RD, A3, CS	Schmitt				1.0	A
	$I_{IH}3$	SP, BUSWD, TIN, TPC1, TPC2, TOSEL1, TOSEL2					1.0	A
Input low-level current	$I_{IL}1$	A0/CL, A1/CE, A2/DI, RST, STNBY	Schmitt		1.0			A
	$I_{IL}2$	IOCNT1, IOCNT2, DACK D0, D1, D2, D3, D4, D5, D6, D7, WR, RD, A3, CS	Schmitt		1.0			A
	$I_{IL}3$	SP, BUSWD, TIN, TPC1, TPC2, TOSEL1, TOSEL2			1.0			A
Output high-level voltage	$V_{OH}1$	CLK16, DATA, FLOCK, BLOCK, FCK, BCK, CRC4	CMOS	I_{OH} = 1 mA	V_{DD} 0.4			V
	$V_{OH}2$	DREQ, RDY, D0, D1, D2, D3, D4, D5, D6, D7, D8, D9, D10, D11, D12, D13, D14, D15, INT	CMOS	I_{OH} = 2 mA	V_{DD} 0.4			V
Output low-level voltage	$V_{OL}1$	CLK16, DATA, FLOCK, BLOCK, FCK, BCK, CRC4	CMOS	I_{OL} = 1 mA			0.4	V
	$V_{OL}2$	DREQ, RDY, D0, D1, D2, D3, D4, D5, D6, D7, D8, D9, D10, D11, D12, D13, D14, D15, INT	CMOS	I_{OL} = 2 mA			0.4	V
	$V_{OL}3$	DO	Nch-Open Drain	I_{OL} = 2 mA			0.4	V
Output leakage current	IOFF	DO		$V_O = V_{DD}$			1.0	A
Hysteresis voltage	VHYS	A0/CL, A1/CE, A2/DI, RST, STNBY, IOCNT1, IOCNT2, DACK, D0, D1, D2, D3, D4, D5, D6, D7, WR, RD, A3, CS				$0.1V_{DD}$		V
Internal feedback resistance	RF	XIN, XOUT				1.0		MΩ
Current drain	I_{DD}					6	12	mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Bandpass Filter Characteristics at Ta = 25 C, V_{DD} = 2.7 V to 3.6 V, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings			unit
			min	typ	max	
Input resistance	RMPX			50		k
Reference supply voltage output	VREF	Vref, Vdda = 3 V		1.5		V
BPF center frequency	FC	FLOUT		76.0		kHz
3 dB band width	FBW	FLOUT		19.0		kHz
Group-delay in band width	DGD	FLOUT			7.5	s
Gain	Gain	FLOUT-MPXIN, f = 76 kHz		20		dB
Attenuation characteristic	ATT1	FLOUT, f = 50 kHz	25			dB
	ATT2	FLOUT, f = 100 kHz	15			dB
	ATT3	FLOUT, f = 30 kHz	50			dB
	ATT4	FLOUT, f = 150 kHz	50			dB

Block Diagram



Pin Assignment

List of Pin Functions

Pin No.	Name of Pin	IO Form	State with RST="L"	Description of Functions
1	XOUT	O	Oscillation	Pin for system clock (crystal oscillator)
2	Vddd	-	-	Digital power pin
3	IOCNT1	I	Input	Data bus I/O control 1 input pin (Parallel IF) * Connect to Vssd when CCB IF (SP=H) is to be used.
4	IOCNT2	I	Input	Data bus I/O control 2 input pin (Parallel IF) * Connect to Vssd when CCB IF (SP=H) is to be used.
5	CLK16	O	L	Clock regeneration monitor pin
6	DATA	O	L	Demodulation data monitor pin
7	FLOCK	O	L	Frame synchronization flag output pin (H: synchronized)
8	BLOCK	O	L	Block synchronization flag output pin (H: synchronized)
9	FCK	O	L	Frame start signal output pin
10	BCK	O	L	Block start signal output pin
11	CRC4	O	H	Layer 4 CRC check result output pin
12	DREQ	O	H	DMA REQ signal output pin (parallel IF)
13	DACK	I	Input	DMA ACK signal input pin (parallel IF) * Connect to Vddd when CCB IF (SP=H) is to be used.
14	Vssd	-	-	Digital GND pin

Continued from preceding page.

Internal Equivalent Circuit of Analog Pins

Name of pin
Pin number in parentheses

CPU Interface <CCB Mode>

CCB (Computer Control Bus), which is the ON Semiconductor original serial bus format for ON Semiconductor's acoustic LSIs, performs data input and output.
The CCB address is transmitted with CE= "L", acknowledging the CCB I/O mode when CE is set to "H".

(1) List of CCB modes

CCB address									I/O mode	Description
Hexadecimal	B0	B1	B2	B3	A0	A1	A2	A3		
FAh	0	1	0	1	1	1	1	1	Input	16-bit control data input
FBh	1	1	0	1	1	1	1	1	Output	Output of data corresponding to the input clock (CL) portion
FCh	0	0	1	1	1	1	1	1	Input	Layer 4 CRC check circuit data input (on the 8-bit units)
Fad	1	0	1	1	1	1	1	1	Output	Output of the register only

(2) Data input (CCB address FAh)

This is to set data to the LSI internal register. DI input includes both CCB address FAh and 16-bit data (DI0 to DI15) are input.

Assignment of each bit is as shown in the table below. Though DI12 to DI15 are invalid data, it is necessary to enter the arbitrary data so that the total of 16 bits can be obtained. For the contents of each register and register address, refer to the chapter of CPU registers.

(Note that writing into the layer 4 CRC check register will be described later (for the CCB address, use FCh.))

(3) Output of the corrected data (CCB address FBh)

The corrected packet data is output from LSI. The CCB address, FBh, is input in DI.

The valid data to be output is maximum 288 bits. If the clock input (CL input) is interrupted halfway to set CE to the "L" level, data output is not troubled by the next interrupt.

The maximum data to be output is 288 bits (36 bytes) and the leading two bytes, to which the status register (STAT) contents and the block number register (BLNO) contents are added, are output.

STAT and BLNO, which are the register contents

Symbol	Parameter	min	typ	max	unit
tCL	Clock “L” level time	0.7			s
tCH	Clock “H” level time	0.7			s
tSU	Data setup time	0.7			s
tHD	Data hold time	0.7			s
tEL	CE wait time	0.7			s
tES	CE setup time	0.7			s
tEH	CE hold time	0.7			s
tLC	Data latch change time			0.7	s
tDDO*1	DO data output time	135		320	ns
TDDO2	DO data output off time	135			ns
tCRC	CRC4 change period			0.7	s

*1 DO data output change time from the “H” level to the “L” level. Output change time from the “L” level to the “H” level is determined by tht.8(t)the “H”

(2) Register output

This is to read data from the register in LSI. Only the status register (STAT) and block number register (BLNO) in LSI can be read.

For accessing, input the register address in A0 to A3, set the CS pin = L, and then the RD pin = L. This causes the RDY pin to change from “H” to “L”. Then, data is output from the D(n) pin after the RDY pin becomes “H”. It is necessary to keep an interval of tCYRD or more before the next data output. (n: 0-7 for BUSWD=L and 0 – 15 for BUSWD=H.)

By setting bit 3 (RDY) = 1 of the control register 2, the RDY pin output method can be changed. In this case, the RDY pin changes from “H” to “L” in the timing enabling output of the acquired data and the pin returns to “H” after the end of data output (shown as Timing 2 in the figure).

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CPU Registers

This LSI has both write registers and read registers. Access to the registers is made via CCB IF or parallel IF. Switching of access mode is made with the SP pin. (CCB IF: SP=H, Parallel IF: SP=L)

(1) Write registers

Setting any data to '0h' or '7h' or larger address of Write-registers is prohibited. Do not set any data to these addresses.

List of write registers

ADR	R/W	Register Name	Description
0h	-	-	Reserved (setting prohibited)
1h	W	BIC	Allowable number of BIC errors
2h	W	SYNCB	Block synchronization: error protection count
3h	W	SYNCF	Frame synchronization: error protection count
4h	W	CTL1	Control register 1
5h	W	CTL2	Control register 2
6h	W	CRC4	Layer 4 CRC register (for the parallel IF only. CCB to use the dedicated address)
7h and beyond	-	-	Reserved (setting prohibited)

1h <BIC>: Number of allowable BIC errors <Write Only>

Register to set the allowable number of BIC error bits for determination of synchronization

ADR	Register Name	Bit	Name	Description	Reset
1h	BIC	7-4	BIC_F	Forward protection value (initial value 2) Sets the allowable number of BIC error bits (when synchronized).	0010b
		3-0	BIC_B	Backward protection value (initial value 2) Sets the number of allowable BIC error bits (when not synchronized).	0010b

When the block synchronization determination output (BLOCK) is to be used determination of whether or not there is

4h <CTL1>: Control register 1 <Write Only>

Register to control the block reset ON/OFF, function activation/stop, and the data output method.

ADR	Register Name	Bit	Name	Description	Reset
4h	CTL1	7	CRC4_RST	Layer 4 CRC check circuit reset setting 1: Reset ON 0: Reset OFF To cancel reset, it is necessary to set 0.	0
		6	DO̅ _MOVE	Sets the DO̅ pin output method changeover 0: Hi-Z state retained in states other than data output 1: Changes in an interlocked manner with the INT signal *6	0
		5	INT_MOVE	Sets changeover of corrected data output method *4 0: Outputs only data received at completion of correction & layer 2 CRC completion as well as during synchronization 1: Outputs all of data	0
		4	SYNC_RST	Synchronization regeneration circuit reset setting *1 1: Reset ON 0: Reset OFF 0 to be set to cancel reset	0
		3	EC_STOP	Error correction function down setting *2 0: All functions activated 1: Only MSK detector circuit and synchronization regeneration circuit activated	0
		2	VEC_HALT	Vertical error correction function down function *3 0: Executes vertical error correction and second horizontal correction. 1: Does not execute vertical error correction and second horizontal correction.	0
		1	RTIB	Real-time information block setting *5 0: Real-time information blocks present. 1: No-real-time information block.	0
		0	FRAME	Frame setting 0: Specifies method B. 1: Specifies method A.	0

*1 With SYNC_RST=1, the synchronization status and the synchronization protection status are cleared, resulting in the unsynchronized state. This function enables rapid pull-in of frame synchronization when the frame synchronization of new tuned and received data is deviated during tuning of a radio receiver. In this case, registers such as the

5h <CTL2>: Control register 2 <Write Only>

Register to control the parallel IF setting, vertically-corrected data output method, etc.

ADR	Register Name	Bit	Name	Description	Reset
5h	CTL2	7	Reserved	Either keep an initial value or set it to 0.	0
		6	BLK_RST	Block synchronization circuit reset setting *1 1: Reset ON 0: Reset OFF 0 to be set to cancel reset	0
		5	DACK	DACK signal polarity setting (effective for SP=L only) 0: Negative logic for DACK signal polarity	

(2) Read registers

List of read registers

ADR	R/W	Register Name	Description
0h	R	PDATO	Input this address into A0 to A3 after reading of error-corrected data
1h	R	STAT	Status register
2h	R	BLNO	Block number register
3h and beyond	-	-	Reserved

Parallel mode: To read registers, send address shown in the list of read registers.
CCB mode: To read registers, send assigned CCB address (FBh or Fad). It is not necessary to send address shown in the list of read registers.

1h <STAT>: Status register <Read Only>
Register to confirm various states

ADR	Register Name	Bit	Name	Description	Reset
1h	STAT	7	VH	Determination on vertically error corrected data 0: Data for which only horizontal correction is performed 1: Data for which vertical and second horizontal correction after horizontal correction are performed	0
		6	BLK	Block synchronization state 0: Data that is received when block synchronization is not established 1: Data that is received when block synchronization is established	0
		5	FRM	Frame synchronization state 0: Data that is received when frame synchronization is not established 1: Data that is received when frame synchronization is established	0
		4	ERR	Error correction state 0: Data whose correction is completed and for which error is not detected by the layer 2 CRC check 1: Data whose correction is impossible or for which error is detected by the layer 2 CRC check.	0
		3	PRI	Determination of parity block 0: Data that is estimated to be data block by the frame synchronization circuit 1: Data that is estimated to be parity block by the frame synchronization circuit	0
		2	HEAD	Frame head determination 1: Data that is estimated to be the frame head block by the frame synchronization circuit 0: Data other than above	0
		1	CRC4	Layer 4 CRC check result 0: Error in layer 4 CRC check result 1: No error in layer 4 CRC check result	1
		0	RTIB	Real-time information block state 1: Indicates the data is a real-time information block.(This bit is valid only in method A'.) 0: The others	0

2h <BLNO>: Block Number register <Read Only>

Register to confirm the output data block Number

ADR	Register Name	Bit	Name	Description	Reset
2h	BLNO	7	BLN7	Indicates the block Number or parity block Number of output data	0
		6	BLN6		0
		5	BLN5	Data block Number 0 to 189	0
		4	BLN4	Parity block Number 0 to 81	0
		3	BLN3		0
		2	BLN2		0
		1	BLN1		0
		0	BLN0		0

The value in the “Reset” column is the readable value immediately after canceling the reset.

Data renewal timing of read register

The timing for rewriting of read register (STAT, BLNO) data is the timing for changing of INT from H to L.

Read procedure of corrected data

Normally, the status register is first read because of occurrence of interrupt to check the condition of corrected output data that is output by the interrupt signal, determining whether or not read is necessary. For example, read is not made till the next interrupt if the error correction result is NG and read is not necessary. r examp(ch)-4.9(eck)-4.9

Error Correction

(1) Error Correction and Output Conditions of Error-corrected Data (in the default state)

The received data is subject to error detection by the layer 2 CRC and error correction by the (272,190) code for each one block (272 bits). At the end of correction, preparation for transmission to CPU is made and the INT signal is output. This is called “horizontal correction”.

In the default state, this INT signal is output only when the output data concerned meets all of three conditions as follows:

Data whose error correction is completed and for which layer 2 CRC detects no error
Data received during block and frame synchronizations
Data in the data packet

*Depending on the register mode setting, horizontally-corrected data may be output regardless of conditions of to above.

When horizontal correction cannot cover completely, correction by the product code is made frame by frame. For data that cannot be horizontally corrected, the second horizontal correction is made.
This series of operations is called “vertical correction”. Conditions for the data obtained from vertically-corrected output are as follows in the default state:

Data that cannot be corrected by horizontal correction, but that has been completely corrected by the vertical correction
Data in the data packet

Accordingly, horizontally-corrected data is not output. Packet data that cannot be corrected horizontally or vertically is not output. The parity packet data after vertical correction is not output either.
Vertical correction is applied to the whole packet data that have been received during frame synchronization, and is executed when horizontal correction cannot correct all packet (block) data. Vertical correction is not made when the error-free data is received for one frame or when the received data is not synchronous in flame synchronization during reception. For the packet whose error has been corrected by horizontal correction and any error-free packet, vertical correction is not made to prevent faulty correction.
In the default setting, the applicable vertically-corrected output is not output when vertical correction has not been made.

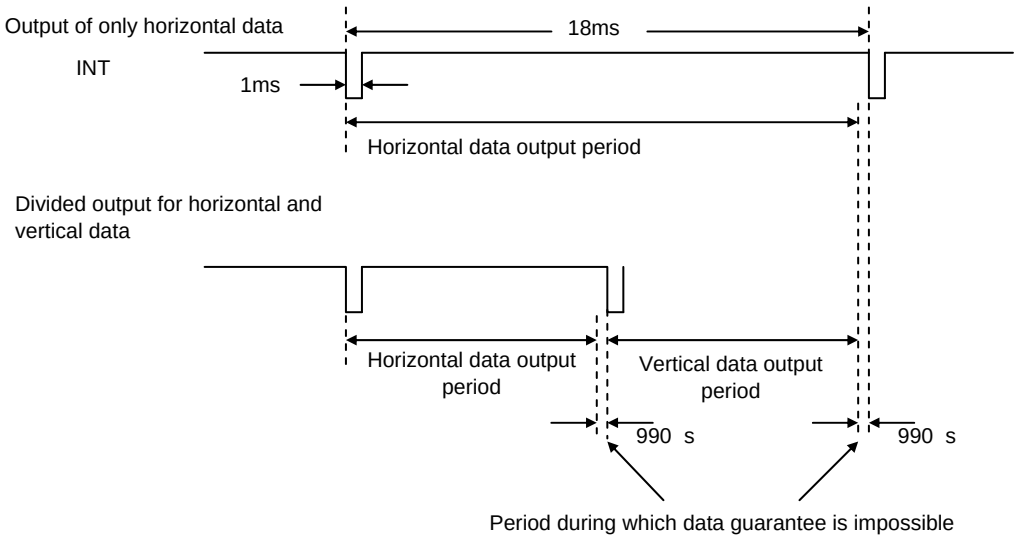
* Depending on the register mode setting, the vertically-corrected data may be output regardless of whether or not vertical correction is to be made.

(2) Error-corrected Data Output Timing (Basic Restrictions)

Data received by LSI is corrected error and written sequentially without any interruption into the output data buffer memory. Since this data buffer memory has a capacity for one-block data, the corrected data before reading is over-written by the next data if data read is delayed. In consequence, it is essential to read data according to the timing stipulations shown below.

This LSI specifies the output timing for each of horizontally and vertically corrected data as follows:

Upon completion of preparation for the output data, LSI lowers the INT pin to “L” as a request for transmission. Data output has the period during which only horizontal data can be read and the period during which horizontal and vertical data are read according to the time division.
Complete data transmission within about 8ms after INT = “L”. When only the horizontally-corrected data can be output, data transmission is possible for about 17ms. Even when CPU is in the course of reading, the output buffer is overwritten by the next output data once the specified time period is expired.
The data amount that can be read by one horizontal and vertical transmission request (INT) is one block only.
Vertically-corrected data is output sequentially beginning with the first block after completion of vertical correction, but the data of parity block is not output.



(3) Horizontally-corrected Data Output Timing (Relationship With The Received Data)

The timing relationship between the received data and interrupt control signal (INT) for horizontary-corrected data output is shown. But the delay from the actual received signal caused by demodulation in

(5) List of Operation Modes

Depending on the set value of INT_MOVE (bit 5 of control register 1) and VEC_OUT (bit 2 of control register 2), the INT signal output timing and output data are modified. In the table below, indicates “output”, indicates “no output.” and - indicates “none applicable.”

Parameter	INT_MOVE	VEC_OUT	Horizontal correction result	Horizontally-corrected output			Vertically-corrected output	
				OK data	NG data	Parity	OK data	NG data
Default value	0	0	OK		-			-
			NG				*1	
Mode 1	1	1	OK		-			