LC72720YV

RDS/RBDS Single-chip Signal Processor IC

ON Semiconductor®

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Overview

The LC72720YV is a single-chip system IC that implement the signal processing required by the European Broadcasting Union RDS (Radio Data System) standard and by the US NRSC (National Radio System Committee) RBDS (Radio Broadcast Data System) standard. This IC include band-pass filter, demodulator, synchronization, and error correction circuits as well as data buffer RAM on chip and perform effective error correction using a soft-decision error correction technique.

Functions

Band-pass filter : switched capacitor filter (SCF)
Demodulator : RDS data clock regeneration and demodulated data reliability information
Synchronization : Block synchronization detection
(with variable backward and forward protection conditions)
Error correction : Soft-decision/hard-decision error correction
Buffer RAM : Adequate for 24 blocks of data (about 500 ms) and flag memory
Data I/O : CCB* interface (power on reset)

Features

Error correction capability improved by soft-decision error correction
The load on the control microprocessor can be reduced by storing decoded data in the on-chip data buffer RAM.
Two synchronization detection circuits provide continuous and stable detection of the synchronization.
Data can be read out starting with the backward-protection block data

* Computer Control Bus (CCB) is an ON Semiconductor's original bus format and the bus addresses are controlled by ON Semiconductor.

ORDERING INFORMATION

See detailed ordering and shipping information on page 19 of this data sheet.

July 2017 - Rev. 1
Publication Order Number :
LC72720YV/D

Specifications

Absolute Maximum Ratings at Ta = 25 C, Vssd = Vssa = 0 V

Parameter	Symbol	Pin Name	Ratings	Unit
Maximum supply voltage	Vddmax	Vddd, Vdda	0.3 to +7.0	V
Maximum input voltage	Vin1max	CL, DI, CE, SYR, T1, T2, T3, T4, T5, T6, T7, SYNC	0.3 to +7.0	V
	Vin2max	XIN	0.3 to Vddd+0.3	V
	Vin3max	MPXIN, CIN	0.3 to Vdda+0.3	V
Maximum output voltage	Vo1max	DO, SYNC, RDS-ID, T3, T4, T5, T6, T7	0.3 to +7.0	V
	Vo2max	XOUT	0.3 to Vddd+0.3	V
	Vo3max	FLOUT	0.3 to Vdda+0.3	V
Maximum output current	Io1max	DO, T3, T4, T5, T6, T7	+6.0	mA

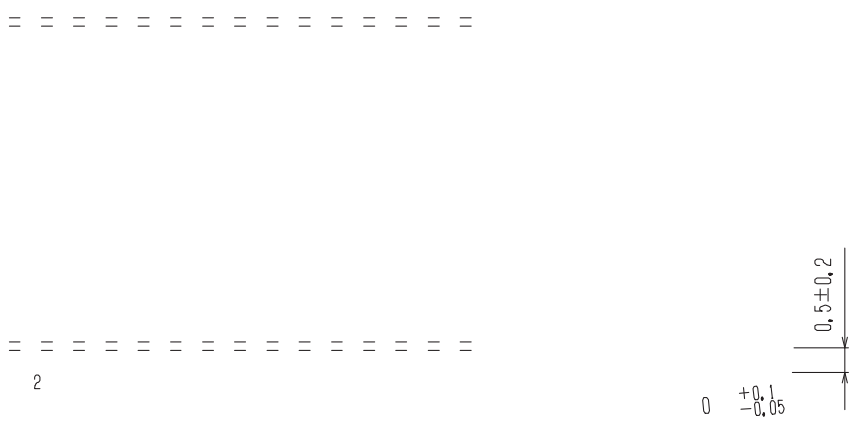
Electrical Characteristics at Ta = 40 to +85 C, Vssd = Vssa = 0 V

Parameter	Symbol	Pin Name	Conditions	Ratings			Unit
				min	typ	max	
Input resistance	R_{MPXIN}	MPXIN-Vssa	f = 0 to 100 kHz		23		kΩ
Internal feedback resistance	Rf	XIN			1.5		MΩ
Center frequency	fc	FLOUT		56.5	57.0	57.5	kHz
3 dB band width	$BW_{3\ dB}$	FLOUT		2.5	3.0	3.5	kHz
Gain	Gain	MPXIN-FLOUT	f = 57 kHz	28	31	34	dB
Stop band Attenuation	Att1	FLOUT	f = 7 kHz	30			dB
	Att2	FLOUT	f < 45 kHz, f > 70 kHz	40			dB
	Att3	FLOUT	f < 20 kHz	50			dB
Group delay deviation							

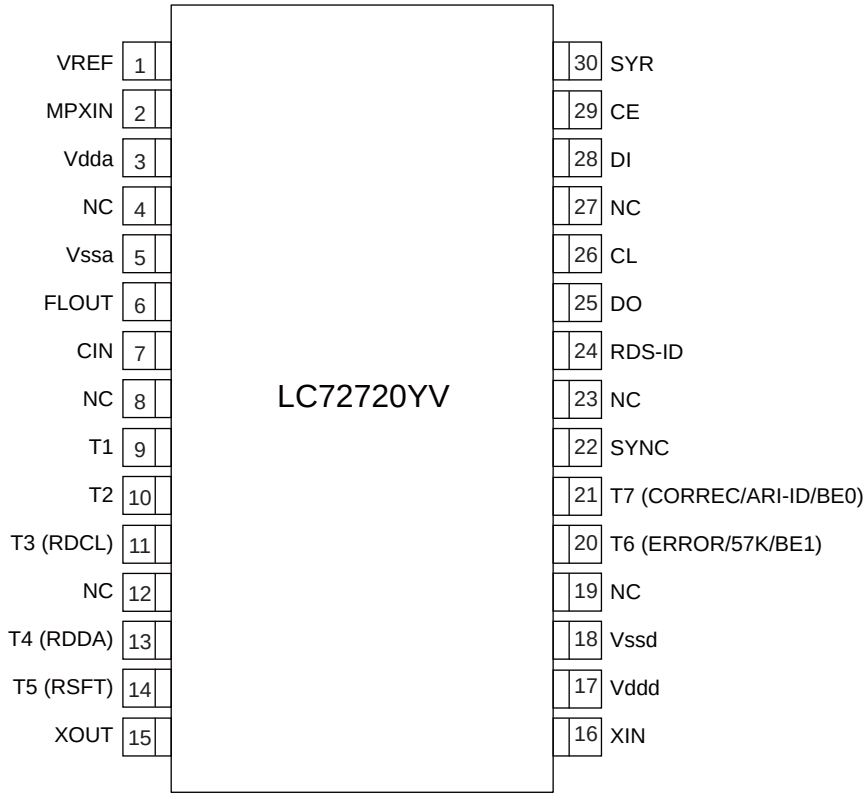
Package Dimensions

unit : mm

SSOP30 (275mil)
CASE 565AT
ISSUE A

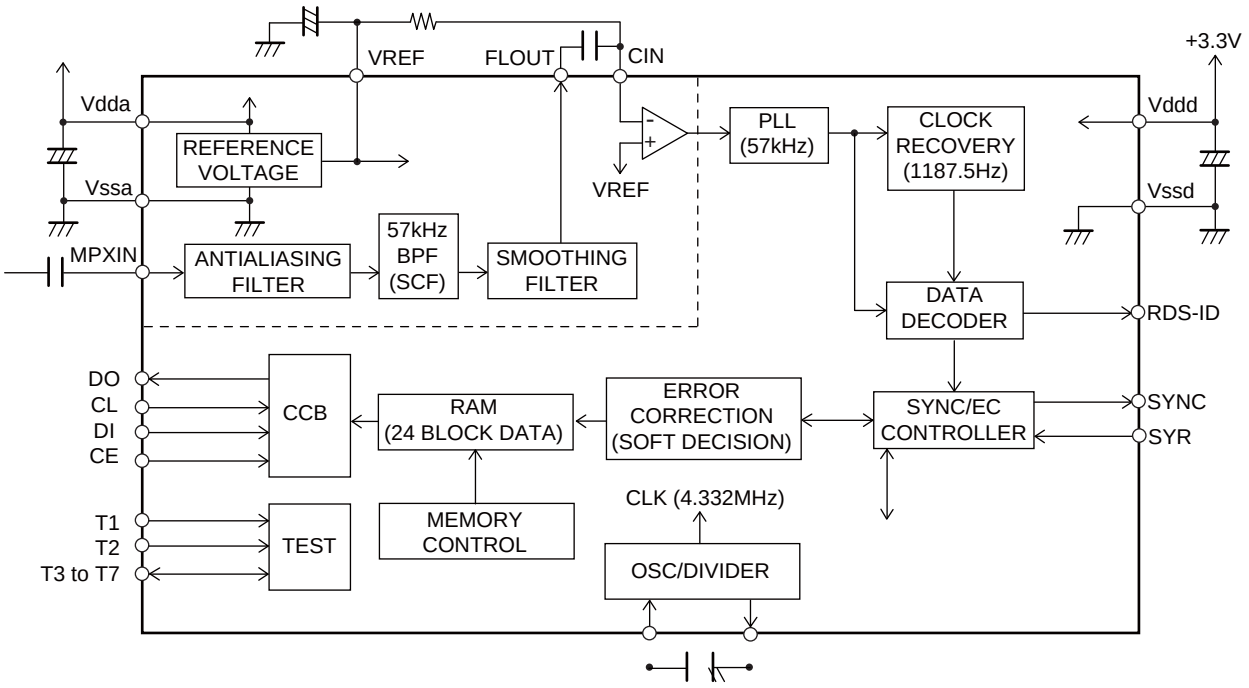


Pin Assignment



Top view

Block Diagram



Pin Functions

CCB output data format

1. Each block of output data consists of 32 bits (4 bytes), of which 2 bytes are RDS data and 2 bytes are flag data.
2. Any number of 32-bits output data blocks can be output consecutively.
3. When there is no data that can be read out in the internal memory, the system outputs blocks of all-zero data consecutively.
4. If data readout is interrupted, the next read operation starts with the 32-bit data block whose readout was interrupted. However, if only the last bit is remaining to be read, it will not be possible to re-read that whole block.
5. The check bits (10 bits) are not output.
6. The data valid (OWD) must not be referred to.
7. When the first leading bits are not “1010”, the read in data is in invalid, and read operation is cancelled.

(1) Offset word detection flag (1bit) : OWD

OWD	Offset word detection
1	Detected
0	Not detected (protection function operating)

(3) Consecutive RAM read out possible flag (1 bit) : RE

RE	RAM data information
1	The next data to be read out is in RAM
0	This data item is the last item in RAM, ant the next data is not present.

(4) RAM data remaining flag (2 bits) : RF0,RF1

RF1	RF0	Remaining data in RAM (number of blocks)
0	0	1 to 7
0	1	8 to 15
1	0	16 to 23
1	1	24

Caution : This value is only meaningful when RE is 1. When RE is 0, there is no data in RAM, even if RF is 00.
If a synchronization reset was applied using SYR, then the backward protection block data that was written to memory is also counted in this value.

(5) ARI(SK) detection flag (1 bit) : ARI

ARI	SK signal
1	Detected
0	Not detected

(6) Synchronization established flag (1 bit) : SYC

SYC	Synchronization detection
1	Synchronized
0	Not synchronized

Caution : This flag indicates the synchronization state of the circuit at the point when the data block being output was received.
On the other hand, the SYNC pin (pin18) output indicates the current synchronization state of the circuit.

(7) Error information flags (3 bits) : E0 to E2

E2	E1	E0	Number of bits corrected
0	0	0	0 (no errors)
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5

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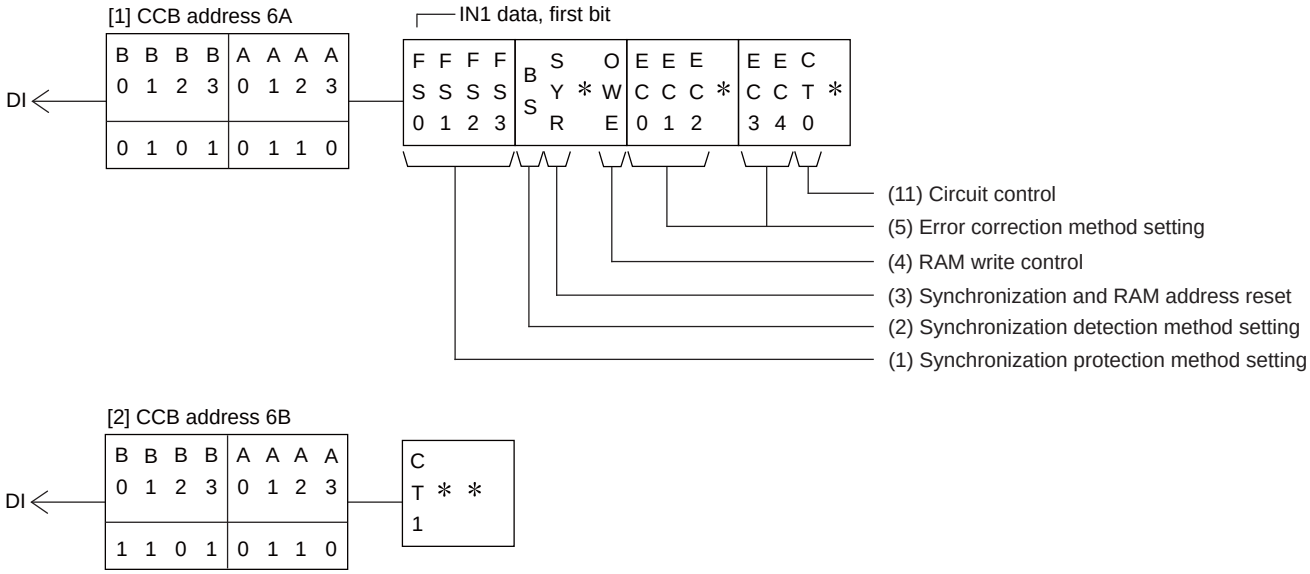
CCB Input data format



(1) Synchronization protection (forward protection) method setting (4 bits) : FS0 to FS3

FS3 = 0 : If offset words in the correct order could not be detected continuously during the number of blocks specified by FS0 to FS2, take that to be a lost synchronization sate.

FS3 = 1 : If blocks with uncorrectable errors were received consecutively during the number of blocks specified by FS0 to FS2, take that to be a lost synchronization state.

FS0	FS1	FS2	Condition for detecting lost synchronization
0	0	0	If 3 consecutive blocks matching the FS3 condition are received.
1	0	0	If 4 consecutive blocks matching the FS3 condition are received.
0	1	0	If 5 consecutive blocks matching the FS3 condition are received.
1	1	0	If 6 consecutive blocks matching the FS3 condition are received.
0	0	1	If 8 consecutive blocks matching the FS3 condition are received.
1	0	1	If 10 consecutive blocks matching the FS3 condition are received.
0	1	1	If 12 consecutive blocks matching the FS3 condition are received.
1	1	1	If 16 consecutive blocks matching the FS3 condition are received.

Initial value : FS0 = 0, FS1 = 1, FS2 = 0, FS3 = 0

(2) Synchronization detection method setting (1 bit) : BS

BS	Synchronization detection conditions
0	If during 3 blocks, 2 blocks of offset words were detected in the correct order.
1	If the offset words were detected in the correct order in 2 consecutive blocks.

Initial value : BS = 0

(3) Synchronization and RAM address reset (1 bit) : SYR

SYR	Synchronization detection circuit	RAM
0	Normal operation (reset cleared)	Normal write (See the description of the OWE bit)
1	Forced to the unsynchronized state (synchronization reset)	After the reset is cleared, start writing from the data prior to the establishment of synchronization, i.e. the data in backward protection.

Initial value : SYR = 0

Caution : 1. To apply a synchronization reset, set SYR to 1 temporarily using CCB, and then set it back to 0 again using CCB. The circuit will start synchronization capture operation at the point SYR is set to 0.

2. The SYR pin (pin30) also provides an identical reset control operation. Applications can use either method. However, the control method that is not used must be set to 0 at all times.
Any pulse with a width of over 250 ns will suffice.

3. A reset must be applied immediately after the reception channel is changed.
If a reset is not applied, reception data from the previous channel may remain in on-chip memory.

4. Data read out after a synchronization reset is read out starting with the backward protection block data preceding the establishment of synchronization.

(4) RAM write control (1 bit) : OWE

OWE	RAM write conditions
0	Only data for which synchronization had been established is written.
1	Data for which synchronization not has been established (unsynchronized data) is also written. (However, this applies when SYR = 0.)

Initial value : OWE = 0

(5) Error correction method setting (5bits) : EC0 to EC4

EC0	EC1	EC2	Number of bits corrected
0	0	0	0 (error detection only)
1	0	0	1 or fewer bits
0	1	0	2 or fewer bits
1	1	0	3 or fewer bits
0	0	1	4 or fewer bits
1	0	1	5 or fewer bits

Initial values : EC0 = 0, EC1 = 1, EC2 = 0, EC3 = 0, EC4 = 1

Caution : 1. If soft-decision A or soft-decision B is specified, soft-decision control will be performed even if the number of bits corrected is set to 0 (error detection only). With these settings, data will be output for blocks with no errors.

2. As opposed to soft-decision B, the soft-decision A setting suppresses soft decision error correction.

(6) Crystal oscillator frequency selection (1 bit) : XS

XS = 0 : 4.332 MHz (Initial value : XS = 0)
XS = 1 : 8.664 MHz

(7) Demodulation circuit phase control (2 bits) : PL0, PL1

PL0	PL1	Demodulation circuit phase control
0	0/1	Normal operation when ARI presence or absence is unclear.
1	0	If the circuit determines that the ARI signal is absent : 90 phase
	1	If the circuit determines that the ARI signal is present : 0 phase

Initial values : PL0 = 0, PL1 = 1

Caution : 1. When PL0 is 0 (normal operation), the IC detects the presence or absence of the ARI signal and reproduces the RDS data by automatically controlling the demodulation phase with respect to the reproduced carrier. However, the initial phase

Item	Pin T3 (RDCL)
PT2 = 0	Data(RDDA and RSFT) changes on this pin's rising edge
PT2 = 1	Data(RDDA and RSFT) changes on this pin's falling edge

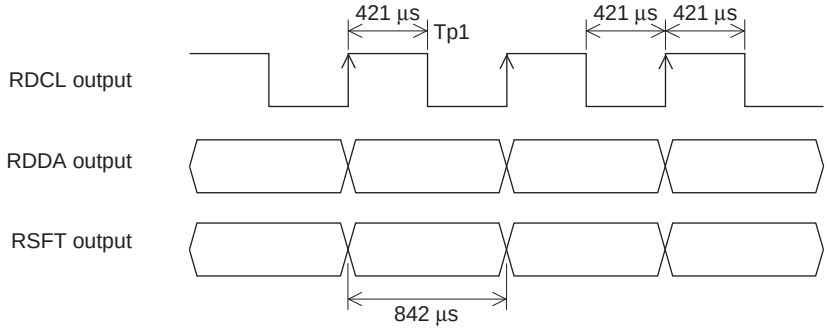
Mode2 (PT2 = 0)	Pin T7 (ARI-ID)
No SK	High (1)
SK present	Low (0)

Mode3 (PT2 = 0)	Pin T6 (ERROR)	Pin T7 (CORREC)
Correction not possible	Low (0)	Low (0)
Errors corrected	High (1)	Low (0)
No errors	High (1)	High (1)

Mode = 4 Number of error blocks (B)	Pin T6 (BE1)	Pin T7 (BE0)
B=0	Low (0)	Low (0)
1 B 20	Low (0)	High (1)
20 B 40	High (1)	Low (0)
40 B 48	High (1)	High (1)

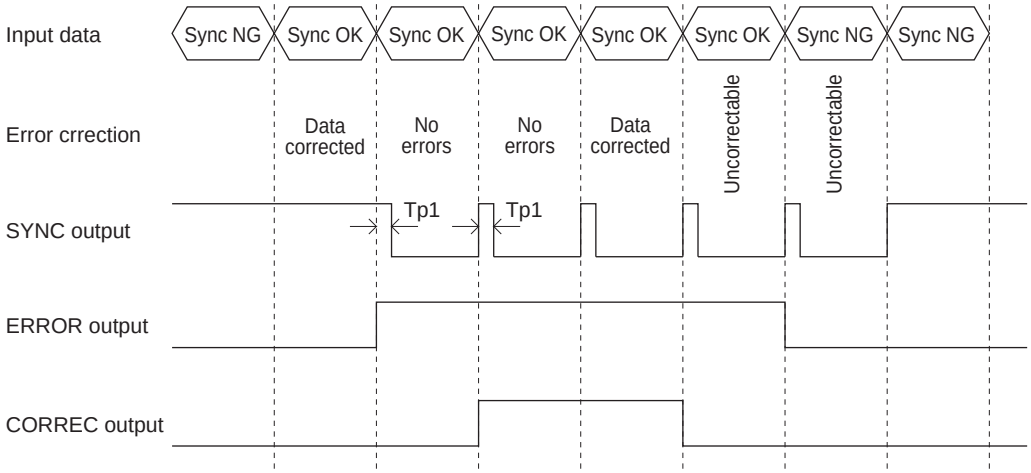
RDCL / RDDA / RSFT and ERROR / CORREC / SYNC output timing

(1) Timing 1



Note : When PT2 = 0, RDDA and RSFT must be acquired on the falling edge of RDCL.

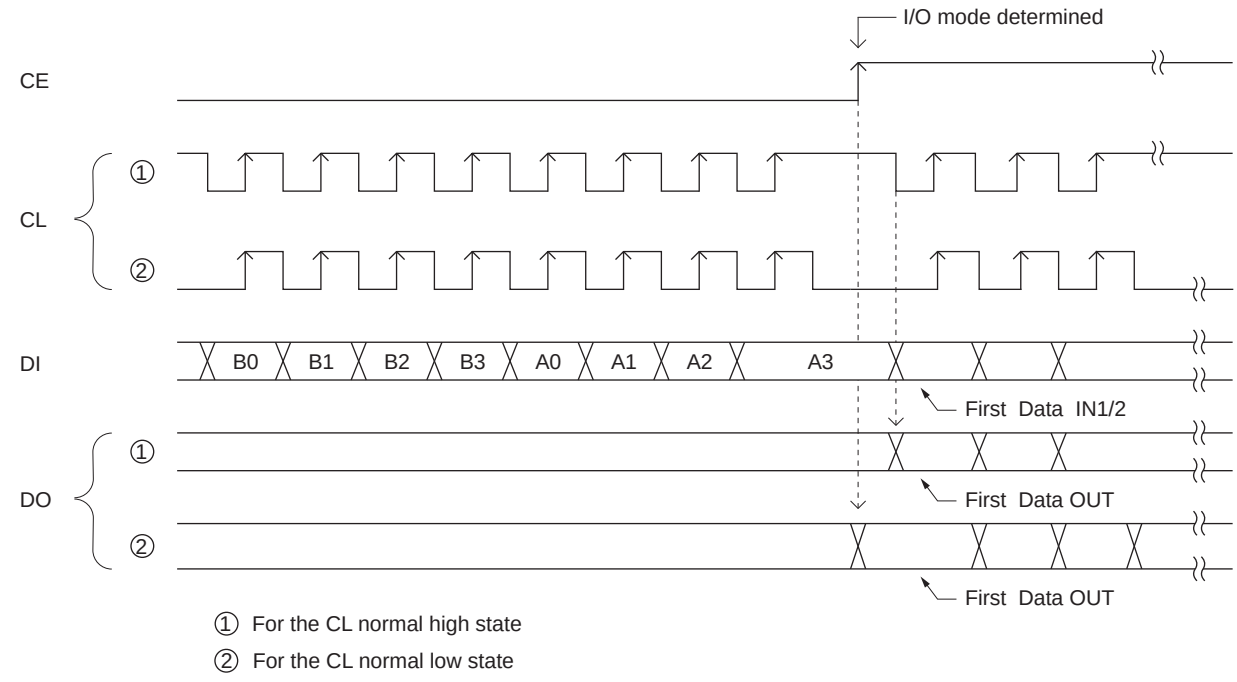
(2) Timing 2 (mode 3, PT2 = 0)



Serial Data Input and Output Methods

Data is input and output using the CCB (Computer Control Bus), which is Our audio IC serial bus format.
This IC adopts an 8-bit address CCB format.

	I/O mode	(LSB) Address (MSB)								Comment
		B0	B1	B2	B3	A0	A1	A2	A3	
[1]	IN1 (6A)	0	1	0	1	0	1	1	0	Control data input mode, also referred to as " serial data input " mode. 16bit data input mode
[2]	IN2 (6B)	1	1	0	1	0	1	1	0	
[3]	OUT (6C)	0	0	1	1	0	1	1	0	Data output mode The data for multiple blocks can be output sequentially in this mode.



(1) Serial data input (IN1 / IN2)

t_{SU}, t_{HD}, t_{EL}, t_{ES}, t_{EH} 0.75 s t_{LC} 1.15 s t_{CE} 20 ms

CL : Normal high

CL : Normal low

(2) Serial data output (OUT)

t_{SU}, t_{HD}, t_{EL}, t_{ES}, t_{EH} 0.75 s t_{DC}, t_{DH} 0.46 s t_{CE} 20 ms

CL : Normal high

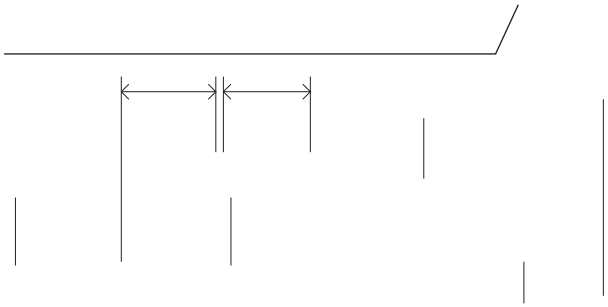
CL : Normal low

Cautions : 1. Since the DO pin is an n-channel open-drain output, the transition times (t_{DC}, t_{DH}) will differ with the value of the pull-up resistor used.

(3) Serial data timing

CL : Normal high

CL : Normal low



Parameter	Symbol	Conditions		min	typ	max	Unit
Data setup time	t_{SU}	DI, CL		0.75			s
Data hold time	t_{HD}	DI, CL		0.75			s
Clock low level time	t_{CL}	CL		0.75			s
Clock high level time	t_{CH}	CL		0.75			s
CE wait time	t_{EL}	CE, CL		0.75			s
CE setup time	t_{ES}	CE, CL		0.75			s
CE hold time	t_{EH}	CE, CL		0.75			s
CE high level time	t_{CE}	CE				20	ms
Data latch transition time	t_{LC}					1.15	s
Data output time	t_{DC}	DO, CL	Differs with the value of the pull-up resistor used.			0.46	s
	t_{DH}	DO, CE				0.46	s

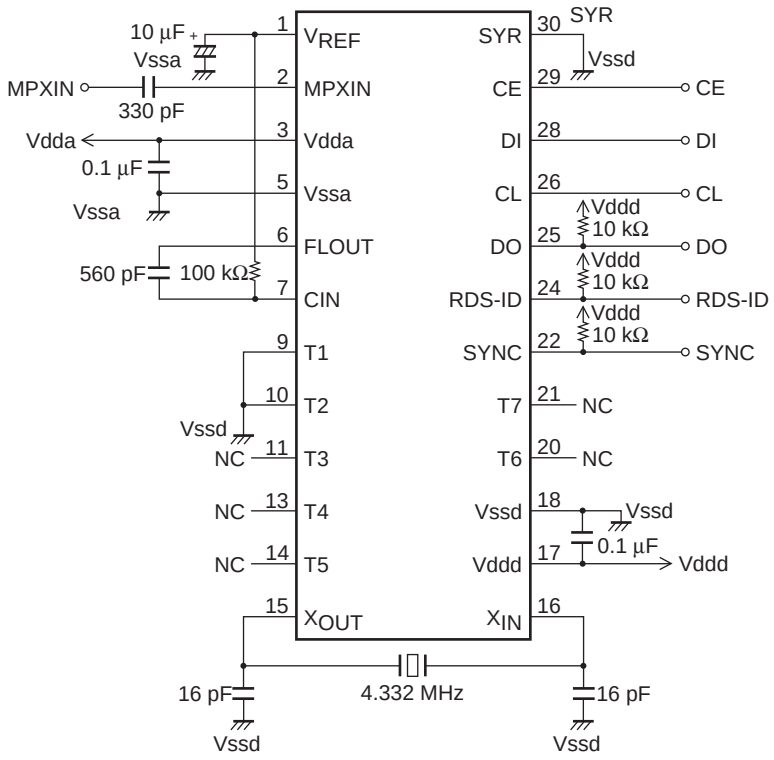
DO pin operation

This IC incorporates a RAM data buffer that can hold up to 24 blocks of data. At the point when one block of data is written to this RAM, the IC issues a read request by switching the DO pin from high to low.
The DO pin always goes high for a fixed period (Tdo = 265 s) after a readout and CE goes low. When all the data in the data buffer has been read out, the DO pin is held in the high state until a new block of data has been written to the RAM. If there is data that has not yet been read remaining in the data buffer, the DO pin goes low after the Tdo time has elapsed.
After a synchronization reset, the DO pin is held high until synchronization is established. It goes low at the point the IC synchronizes.

When the DO pin is high following the 265 s period (Tdo) after data is read out.
Here, the buffer is in the empty state, i.e. the state where new data has not been written. After this, when the DO pin goes low, applications are guaranteed to be able to read out that data without it being overwritten by new data if they start a readout operation within 480 ms of DO going low.

When DO goes low 265 s after data is read out
Here, there is data that has not been read out remaining in the data buffer. In this case, applications are guaranteed to be able to read out that data without it being overwritten by new data if they start a readout

Sample Application circuit



Caution : 1. Determine the value of the DO pin pull-up resistor based on the required serial data transfer speed.
2. A 100-k bias resistor must be connected between the CIN pin and the VREF pin. Note that this resistor is planned to be included internally to the IC in later versions of this product.
3. If the SYR pin is unused, it must be connected to ground.

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LC72720YV-TLM-E	SSOP30 (275 mil) (Pb-Free)	1000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D. http://www.onsemi.com/pub_link/Collateral/BRD8011-D.PDF