LC72720YVS

RDS/RBDS Single-chip Signal Processor IC

ON Semiconductor®

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Overview

The LC72720YVS is a single-chip system IC that implement the signal processing required by the European Broadcasting Union RDS (Radio Data System) standard and by the US NRSC (National Radio System Committee) RBDS (Radio Broadcast Data System) standard. This IC include band-pass filter, demodulator, synchronization, and error correction circuits as well as data buffer RAM on chip and perform effective error correction using a soft-decision error correction technique.

Functions

Band-pass filter : switched capacitor filter (SCF)
Demodulator : RDS data clock regeneration and demodulated data reliability information
Synchronization : Block synchronization detection
(with variable backward and forward protection conditions)
Error correction : Soft-decision/hard-decision error correction
Buffer RAM : Adequate for 24 blocks of data (about 500 ms) and flag memory
Data I/O : CCB* interface (power on reset)

* Computer Control Bus (CCB) is an ON Semiconductor's original bus format and the bus addresses are controlled by ON Semiconductor.

ORDERING INFORMATION

See detailed ordering and shipping information on page 19 of this data sheet.

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Publication Order Number :
LC72720YVS/D

Specifications

Absolute Maximum Ratings at Ta = 25 C, Vssd = Vssa = 0 V

Parameter	Symbol	Pin Name	Ratings	Unit
Maximum supply voltage	Vddmax	Vddd, Vdda	0.3 to +7.0	V
Maximum input voltage	Vin1max	CL, DI, CE, SYR, T1, T2, T3, T4, T5, T6, T7, SYNC	0.3 to +7.0	V
	Vin2max	XIN	0.3 to Vddd+0.3	V
	Vin3max	MPXIN, CIN	0.3 to Vdda+0.3	V
Maximum output voltage	Vo1max	DO, SYNC, RDS-ID, T3, T4, T5, T6, T7	0.3 to +7.0	V
	Vo2max	XOUT	0.3 to Vddd+0.3	V
	Vo3max	FLOUT	0.3 to Vdda+0.3	V
Maximum output current	Io1max	DO, T3, T4, T5, T6, T7	+6.0	mA
	Io2max	XOUT, FLOUT	+3.0	mA
	Io3max	SYNC, RDS-ID	+20.0	mA
Allowable power dissipation	Pdmax	(Ta 85 C)	150	mW
Operating temperature	Topr		40 to +85	C
Storage temperature	Tstg		55 to +125	C 25 q

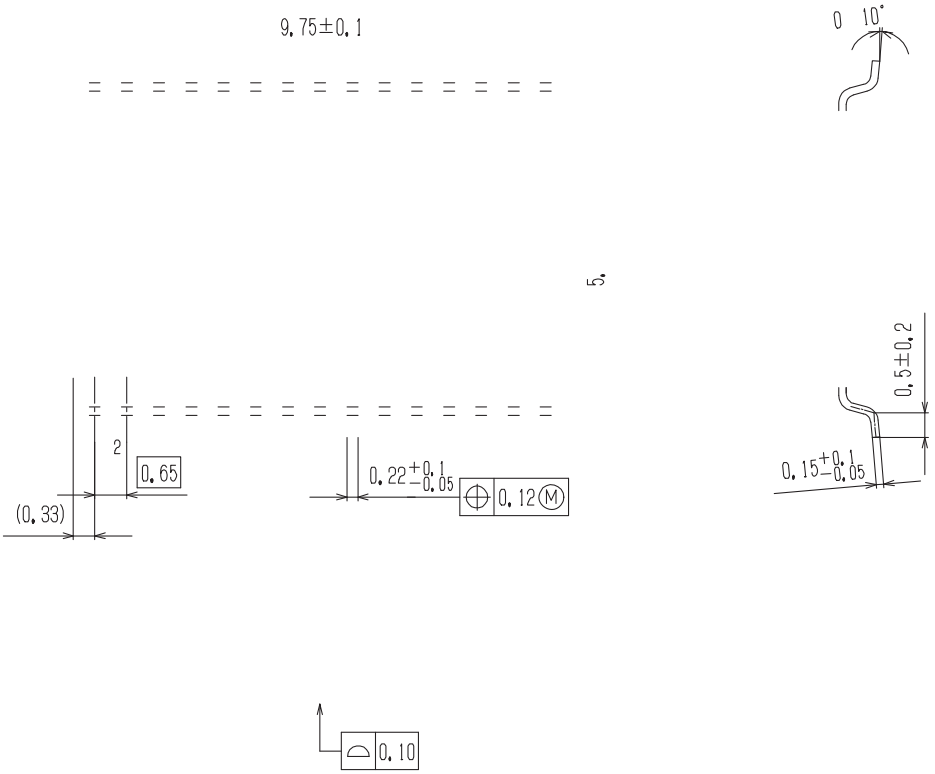
Electrical Characteristics at Ta = 40 to +85 C, Vssd = Vssa = 0 V

Parameter	Symbol	Pin Name	Conditions	Ratings			Unit
				min	typ	max	
Input resistance	R_{MPXIN}	MPXIN-Vssa	f = 0 to 100 kHz		23		kΩ
Internal feedback resistance	Rf	XIN			1.5		MΩ
Center frequency	fc	FLOUT		56.5	57.0	57.5	kHz
3 dB band width	$BW_{3\ dB}$	FLOUT		2.5	3.0	3.5	kHz
Gain	Gain	MPXIN-FLOUT	f = 57 kHz	28	31	34	dB
Stop band Attenuation	Att1	FLOUT	f = 7 kHz	30			dB
	Att2	FLOUT	f < 45 kHz, f > 70 kHz	40			dB
	Att3	FLOUT	f < 20 kHz	50			dB
Group delay deviation	G-Delay	FLOUT	f = 57 1.2 kHz			2.0	s
Reference voltage output	Vref	Vref	Vdda = 5.0 V		1.65		V
Hysteresis	V_{HIS}	CL, DI, CE, SYR, T1, T2			0.1Vddd		V
Output low-level voltage	V_{OL1}	DO, T3, T4, T5, T6, T7	I = 2 mA			0.5	V
	V_{OL2}	SYNC, RDS-ID	I = 8 mA			0.5	V
Input high-level current	I_{IH1}	CL, DI, CE, SYR, T1, T2	V_I = Vddd			5.0	A
	I_{IH2}	XIN	V_I = Vddd	I_{IH1}			

Package Dimensions

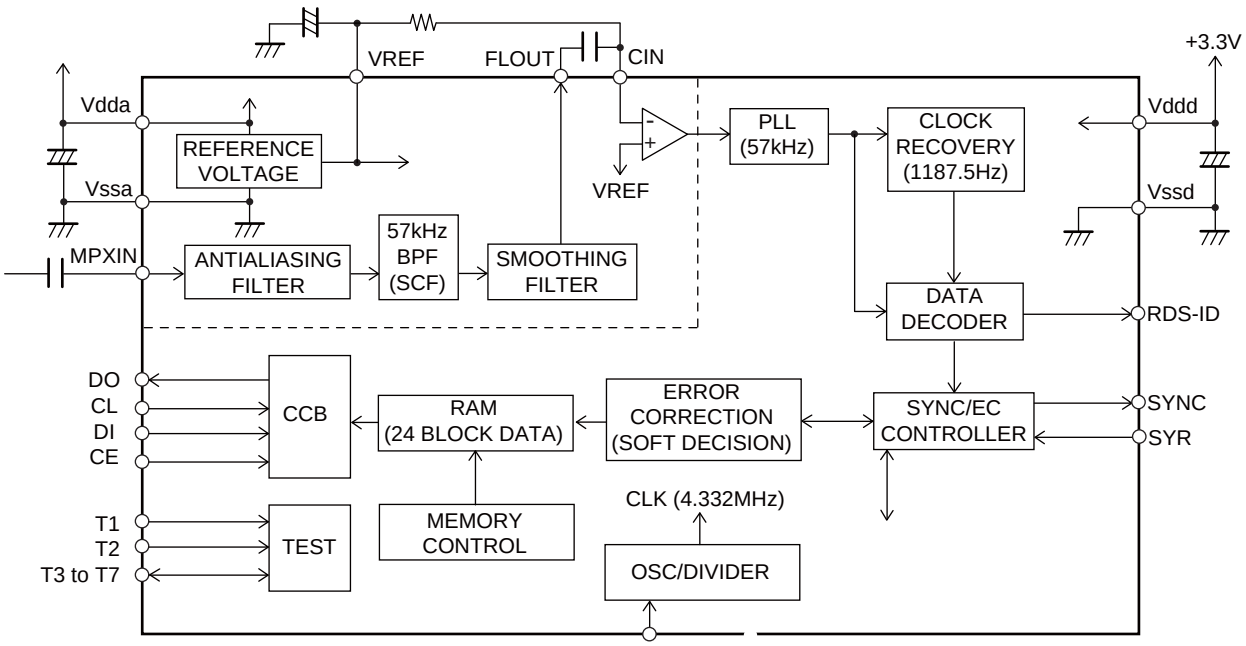
unit : mm

SSOP30 (275mil)
CASE 565AT
ISSUE A



Pin Assignment

Block Diagram



Pin Functions

Pin No.	Pin name	Function	I/O	Pin circuit
1	VREF	Reference voltage output (Vdda/2)	Output	
2	MPXIN	Baseband (multiplexed) signal input	Input	
6	FLOUT	Subcarrier output (filter output)	Output	
7	CIN	Subcarrier input (comparator input)	Input	
3	Vdda	Analog system power supply (+3.3 V)		
5	Vssa	Analog system ground		
15	XOUT	Crystal oscillator output (4.332 / 8.664 MHz)	Output	
16	XIN	Crystal oscillator input (external reference signal input)	Input	
9	T1	Test input (This pin must always be connected to ground.)		
10	T2	Test input (standby control) 0:Normal operation, 1:Standby state (crystal oscillator stopped)		
11	T3(RDCL)	Test I/O (RDS clock output)	I/O*	
13	T4(RDDA)	Test I/O (RDS data output)		
14	T5(RSFT)	Test I/O (soft-decision control data output)		
20	T6 (ERROR/57K/BE1)	Test I/O (error status, regenerated carrier, error block count)		
21	T7 (CORREC/ARI-ID/BE0)	Test I/O (error correction status, SK detection, error block count)		
22	SYNC	Block synchronization detection output		
24	RDS-ID	RDS detection output	Output	
25	DO	Data output		
26	CL	Clock input	Input	
28	DI	Data input		
29	CE	Chip enable		
30	SYR	Synchronization and RAM address reset (active high)		
17	Vddd	Digital system power supply (+3.3 V)		
18	Vssd	Digital system ground		

CCB output data format

1. Each block of output data consists of 32 bits (4 bytes), of which 2 bytes are RDS data and 2 bytes are flag data.
2. Any number of 32-bits output data blocks can be output consecutively.
3. When there is no data that can be read out in the internal memory, the system outputs blocks of all-zero data consecutively.
4. If data readout is interrupted, the next read operation starts with the 32-bit data block whose readout was interrupted. However, if only the last bit is remaining to be read, it will not be possible to re-read that whole block.
5. The check bits (10 bits) are not output.
6. The data valid (OWD) must not be referred to.
7. When the first leading bits are not “1010”, the read in data is in invalid, and read operation is cancelled.

(1) Offset word detection flag (1 bit) : OWD

OWD	Offset word detection
1	Detected
0	Not detected (protection function operating)

(3) Consecutive RAM read out possible flag (1 bit) : RE

RE	RAM data information
1	The next data to be read out is in RAM
0	This data item is the last item in RAM, ant the next data is not present.

(4) RAM data remaining flag (2 bits) : RF0,RF1

CCB Input data format

(1) Synchronization protection (forward protection) method setting (4 bits) : FS0 to FS3

FS3 = 0 : If offset words in the correct order could not be detected continuously during the number of blocks specified by FS0 to FS2, take that to be a lost synchronization sate.

FS3 = 1 : If blocks with uncorrectable errors were received consecutively during the number of blocks specified by FS0 to FS2, take that to be a lost synchronization state.

F	F
S	S
0	

(2) Synchronization detection method setting (1 bit) : BS

BS	Synchronization detection conditions
0	If during 3 blocks, 2 blocks of offset words were detected in the correct order.
1	If the offset words were detected in the correct order in 2 consecutive blocks.

Initial value : BS = 0

(6) Crystal oscillator frequency selection (1 bit) : XS

XS = 0 : 4.332 MHz (Initial value : XS = 0)
XS = 1 : 8.664 MHz

(7) Demodulation circuit phase control (2 bits) : PL0, PL1

PL0	PL1	Demodulation circuit phase control
0	0/1	Normal operation when ARI presence or absence is unclear.
1	0	If the circuit determines that the ARI signal is absent : 90 phase
	1	If the circuit determines that the ARI signal is present : 0 phase

Initial values : PL0 = 0, PL1 = 1

Caution : 1. When PL0 is 0 (normal operation), the IC detects the presence or absence of the ARI signal and reproduces the RDS data by automatically controlling the demodulation phase with respect to the reproduced carrier. However, the initial phase following a synchronization reset is set by PL1.

2. If PL0 is set to 1, the demodulation circuit phase is locked according to the PL1 setting at either 90 (PL1 = 0) or 0 (PL1 = 1), allowing RDS data to be reproduced. When ARI is not present, PL1 should be set to 0, since the RDS data is reproduced by detecting at a phase of 90 with respect to the reproduced carrier. When ARI is present, PL1 should be set to 1, since detection is at 0 . In cases where the ARI presence is known in advance, more stable reproduction can be achieved by fixing the demodulation phase in this manner.

(8) RDS/RBDS(MMBS) selection (1 bit) : RM

RM	RBDS	Decoding method
0	None	Only RDS data is decoded correctly (Offset word E is not detected.)
1	Provided	RDS and MMBS data is decoded correctly (Offset word E is also detected.)

Initial value : RM=0

(9) Output pin settings (3 bits) : PT0 to PT2
These bits control the T3, T4, T5, T6, T7, SYNC, and RDS-ID pins

MODE	PT0	PT1	PT2	T3	T4	T5	T6	T7

Item	Pin T3 (RDCL)
PT2 = 0	Data(RDDA and RSFT) changes on this pin's rising edge
PT2 = 1	Data(RDDA and RSFT) changes on this pin's falling edge

Mode2 (PT2 = 0)	Pin T7 (ARI-ID)
No SK	High (1)
SK present	Low (0)

Mode3 (PT2 = 0)	Pin T6 (ERROR)	Pin T7 (CORREC)
Correction not possible	Low (0)	Low (0)
Errors corrected	High (1)	Low (0)
No errors	High (1)	High (1)

Mode = 4 Number of error blocks (B)	Pin T6 (BE1)	Pin T7 (BE0)
B=0	Low (0)	Low (0)
1 B 20	Low (0)	High (1)
20 B 40	High (1)	Low (0)
40 B 48	High (1)	High (1)

These pins indicate the number of blocks in a set of 48 blocks that had errors before correction.
The output polarity of these pins is fixed at the values listed in the table.

Mode (PT2 = 0)	The SYNC pin
0 to 2	When synchronized : Low (0), When unsynchronized: High (1)
3	When synchronized : Goes high for a fixed period (421 s) at the start of a block and then goes low. When unsynchronized : High (1)

Caution : The output indicates the synchronization state for the previous block.

When PT2 = 0	The RDS-ID pin
No RDS	High (1)
RDS present	Low (0)

(10) Test mode settings (4bits) : TS0 to TS3
Initial values : TS0 = 0, TS1 = 0, TS2 = 0, TS3 = 0
(Applications must set these bits to the above values.)

Notes : The T1 and T2 pins (pins 9 and 10) are related to test mode as follows.

Pin T1	Pin T2	IC operation	Notes
0	0	Normal operating mode	These states are user settable
0	1	Standby mode (crystal oscillator stopped)	
1	0/1	IC test mode	Users cannot use this state

The T1 pin must be tied to V_{SS} (0V).

(11) Circuit control (2 bits) : CT0 and CT1

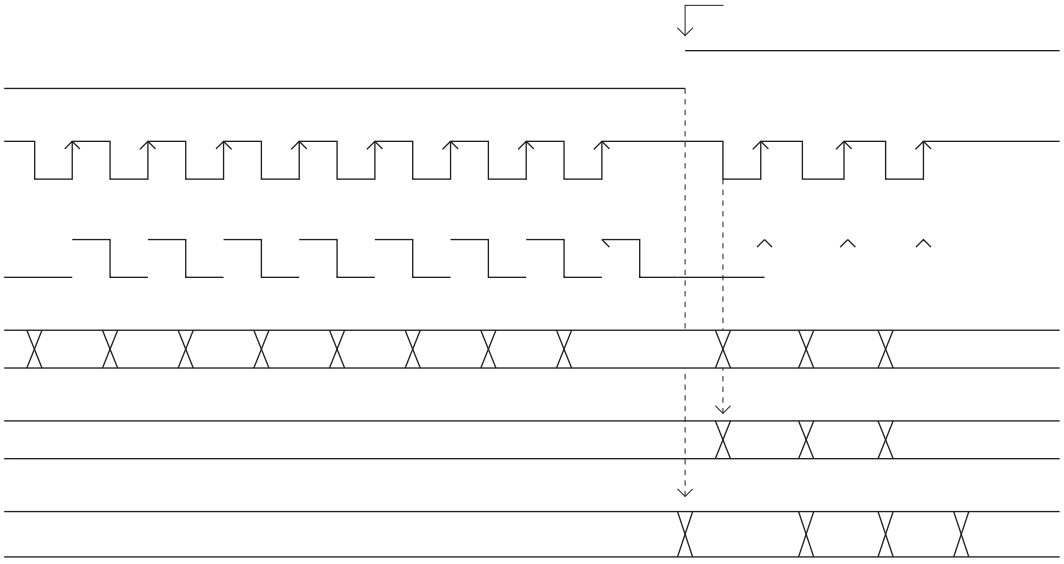
	Item	Control
CT0	RSFT control	When set to 1, soft-decision control data (RSFT) is easier to generate.
CT1	RDS-ID detection condition	When set to 1, the RDS-ID detection conditions are made more restrictive.

Initial value : CT0 = 0, CT1 = 0

Serial Data Input and Output Methods

Data is input and output using the CCB (Computer Control Bus), which is Our audio IC serial bus format.
This IC adopts an 8-bit address CCB format.

	I/O mode	(LSB) Address (MSB)								Comment
		B0	B1	B2	B3	A0	A1	A2	A3	
[1]	IN1 (6A)	0	1	0	1	0	1	1	0	Control data input mode, also referred to as " serial data input " mode. 16bit data input mode
[2]	IN2 (6B)	1	1	0	1	0	1	1	0	
[3]	OUT (6C)	0	0	1	1	0	1	1	0	Data output mode The data for multiple blocks can be output sequentially in this mode.



(1) Serial data input (IN1 / IN2)

t_{SU}, t_{HD}, t_{EL}, t_{ES}, t_{EH} 0.75 s t_{LC} 1.15 s t_{CE} 20 ms

CL : Normal high

(3) Serial data timing

CL : Normal high

CL : Normal low

Parameter	Symbol	Conditions	min	typ	max	Unit
Data setup time	t_{SU}	DI, CL	0.75			s
Data hold time	t_{HD}	DI, CL	0.75			s
Clock low level time	t_{CL}	CL	0.75			s
Clock high level time	t_{CH}	CL	0.75			s

DO pin operation

This IC incorporates a RAM data buffer that can hold up to 24 blocks of data. At the point when one block of data is written to this RAM, the IC issues a read request by switching the DO pin from high to low.
The DO pin always goes high for a fixed period (Tdo = 265 s) after a readout and CE goes low. When all the data in the data buffer has been read out, the DO pin is held in the high state until a new block of data has been written to the RAM. If there is data that has not yet been read rema

Sample Application Circuit

Caution : 1. Determine the value of the DO pin pull-up resist