LC72722PM

RDS / RBDS Single-chip Signal Processor

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Overview

The LC72722PM is a single-chip system IC that implement the signal

* Computer Control Bus (CCB) is an ON Semiconductor's original bus format and the bus addresses are controlled by ON Semiconductor.

ORDERING INFORMATION

See detailed ordering and shipping information on page 18 of this data sheet.

June 2017 - Rev. 2

Publication Order Number :
LC72722PM/D

Specifications

Absolute Maximum Ratings at Ta = 25 C, Vssd = Vssa = 0 V

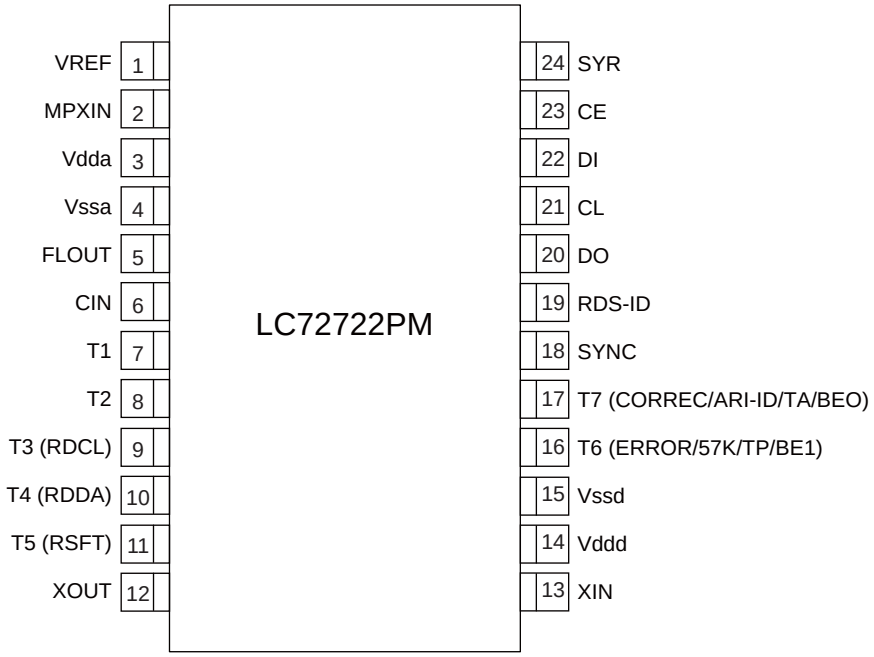
Parameter	Symbol	Pin Name	Ratings	Unit
Maximum supply voltage	Vddmax	Vddd, Vdda	0.3 to +7.0	V
Maximum input voltage	Vin1max	CL, DI, CE, SYR, T1, T2, T3, T4, T5, T6, T7, SYNC	0.3 to +7.0	V
	Vin2max	XIN	0.3 to Vddd+0.3	V
	Vin3max	MPXIN, CIN	0.3 to Vdda+0.3	V
Maximum output voltage	Vo1max	DO, SYNC, RDS-ID, T3, T4, T5, T6, T7	0.3 to +7.0	V
	Vo2max	XOUT	0.3 to Vddd+0.3	V
	Vo3max	FLOUT	0.3 to Vdda+0.3	V
Maximum output current	Io1max	DO, T3, T4, T5, T6, T7	+6.0	mA
	Io2max	XOUT, FLOUT	+3.0	mA
	Io3max	SYNC, RDS-ID	+20.0	mA
Allowable power dissipation	Pdmax	(Ta 85 C)		

Electrical Characteristics at Ta = 40 to 85 C, Vssd = Vssa = 0 V

Parameter	Symbol	Pin Name	Conditions	Ratings			Unit
				min	typ	max	
Input resistance	R_{MPXIN}	MPXIN-Vssa	f = 57 kHz		43.0		kΩ
	Rcin	C_{IN}-Vssa	f = 57 kHz		100.0		kΩ
Internal feedback resistance	Rf	XIN			1.0		MΩ
Center frequency	fc	FLOUT		56.5	57.0	57.5	kHz
3 dB band width	BW_{-3dB}	FLOUT		2.5	3.0	3.5	kHz
Gain	Gain	MPXIN-FLOUT	f = 57 kHz	28	31	34	dB
Stop band Attenuation	Att1	FLOUT	f = 7 kHz	30			dB
	Att2	FLOUT	f < 45 kHz, f > 70 kHz	40			dB
	Att3	FLOUT	f < 20 kHz	50			dB
Reference voltage output	Vref	Vref	Vdda = 5.0 V		2.5		V
Hysteresis	V_{HIS}	CL, DI, CE, SYR, T1, T2			0.1Vddd		V
Output low-level voltage	V_{OL1}	DO, T3, T4, T5, T6, T7	I = 2 mA			0.5	V
	V_{OL2}	SYNC, RDS-ID	I = 8 mA			0.5	V
Input high-level current	I_{IH1}	CL, DI, CE, SYR, T1, T2	V_I = Vddd			5.0	A
	I_{IH2}	XIN	V_I = Vddd	2.0		11.0	A
Input low-level current	I_{IL1}	CL, DI, CE, SYR, T1, T2	V_I = 0 V			5.0	A
	I_{IL2}	XIN	V_I = 0 V	2.0		11.0	A
Output off leakage current	I_{OFF}	DO, SYNC, RDS-ID, T3, T4, T5, T6, T7	V_O = 6.5 V			5.0	A
Current drain	Idd	Vddd, Vdda			9		mA

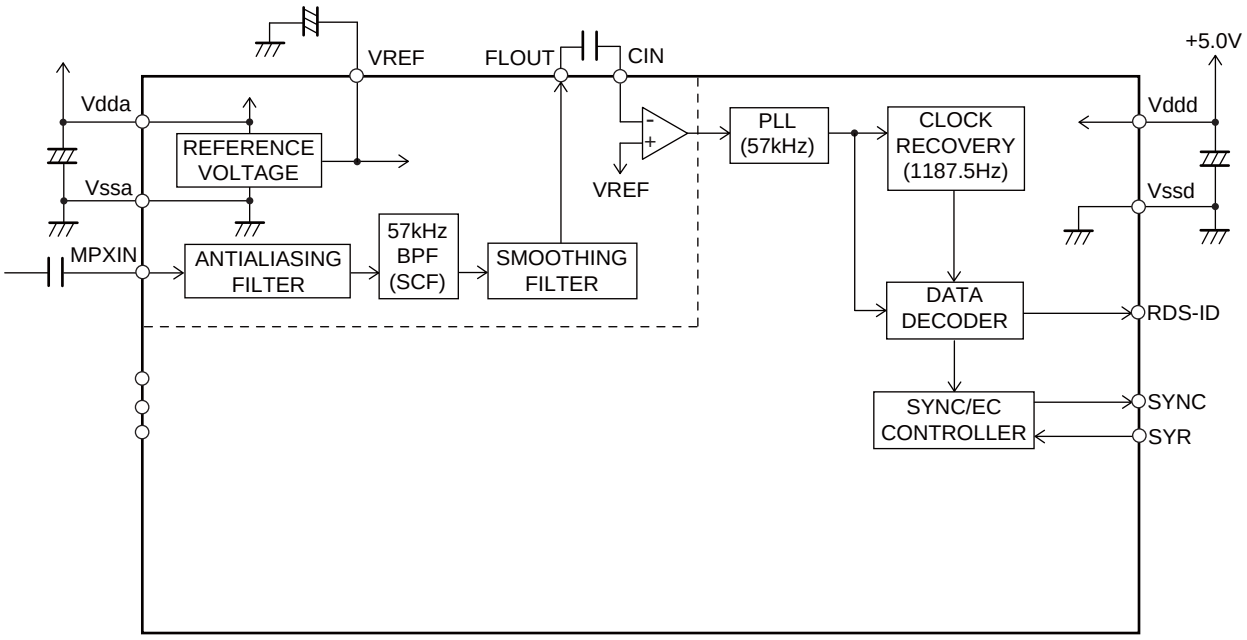
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Pin Assignment



Top view

Block Diagram



Pin Functions

Pin No.	Pin name	Function	I/O	Pin circuit
1	VREF	Reference voltage output (Vdda/2)	Output	
2	MPXIN	Baseband (multiplexed) signal input	Input	
5	FLOUT	Subcarrier output (filter output)	Output	
7	CIN	Subcarrier input (comparator input)	Input	
3	Vdda	Analog system power supply (+5V)		
4	Vssa	Analog system ground		

CCB output data format

1. Each block of output data consists of 32 bits (4 bytes), of which 2 bytes are RDS data and 2 bytes are flag data.
2. Any number of 32-bits output data blocks can be output consecutively.
3. When there is no data that can be read out in the internal memory, the system outputs blocks of all-zero data consecutively.
4. If data readout is interrupted, the next read operation starts with the 32-bit data block whose readout was interrupted. However, if only the last bit is remaining to be read, it will not be possible to re-read that whole block.
5. The check bits (10 bits) are not output.
6. The data valid (OWD) must not be referred to.
7. When the first leading bits are not “1010”, the read in data is in invalid, and read operation is cancelled.

(1) Offset word detection flag (1bit) : OWD

OWD	Offset word detection
1	Detected
0	Not detected (protection function operating)

(2) Offset word information flag (3bit) : B0 to B2

B2	B1	B0	Offset word

(3) Consecutive RAM read out possible flag (1bit) : RE

RE	RAM data information
1	The next data to be read out is in RAM
0	This data item is the last item in RAM, ant the next data is not present.

(3) Synchronization and RAM address reset (1bit) : SYR

SYR	Synchronization detection circuit	RAM
0	Normal operation (reset cleared)	Normal write (See the description of the OWE bit)
1	Forced to the unsynchronized state (synchronization reset)	After the reset is cleared, start writing from the data prior to the establishment of synchronization, i.e. the data in backward protection.

Initial value : SYR = 0

Caution : 1. To apply a synchronization reset, set SYR to 1 temporarily using CCB, and then set it back to 0 again using CCB. The circuit will start synchronization capture operation at the point SYR is set to 0.

2. The SYR pin (pin24) also provides an identical reset control operation. Applications can use either method. However, the control method that is not used must be set to 0 at all times.
Any pulse with a width of over 250 ns will suffice.

3. A reset must be applied immediately after the reception channel is changed.
If a reset is not applied, reception data from the previous channel may remain in on-chip memory.

4. Data read out after a synchronization reset is read out starting with the backward protection block data preceding the establishment of synchronization.

(4) RAM write control (1bit) : OWE

OWE	RAM write conditions
0	Only data for which synchronization had been established is written.
1	Data for which synchronization not has been established (unsynchronized data) is also written. (However, this applies when SYR = 0.)

Initial value : OWE = 0

(5) Error correction method setting (5bits) : EC0 to EC4

Initial values : EC0 = 0, EC1 = 1, EC2 = 0, EC3 = 0, EC4 = 1

Caution : 1. If soft-decision A or soft-decision B is specified, so

Mode1 (PT2 = 0)	Pin T7 (TA)
TA = 0 detected	High (1)
TA = 1 detected	Low (0)

TA = Traffic announcement code

Mode2 (PT2 = 0)	Pin T7 (ARI-ID)
No SK	High (1)
SK present	Low (0)

Mode3 (PT2 = 0)	Pin T6 (ERROR)	Pin T7 (CORREC)
Correction not possible	Low (0)	Low (0)
Errors corrected	High (1)	Low (0)
No errors	High (1)	High (1)

Mode = 4 Number of error blocks (B)	Pin T6 (BE1)	Pin T7 (BE0)
B=0	Low (0)	Low (0)
1 B 20	Low (0)	High (1)
20 B 40	High (1)	Low (0)
40 B 48	High (1)	High (1)

These pins indicate the number of blocks in a set of 48 blocks that had errors before correction.
The output polarity of these pins is fixed at the values listed in the table.

Mode (PT2 = 0)	The SYNC pin
0 to 2	

RDCL / RDDA / RSFT and ERROR / CORREC / SYNC output timing

(1) Timing 1

Note : When PT2 = 0, RDDA and RSFT must be acquired on the falling edge of RDCL.

(2) Timing 2 (mode 3, PT2 = 0)

Serial Data Input and Output Methods

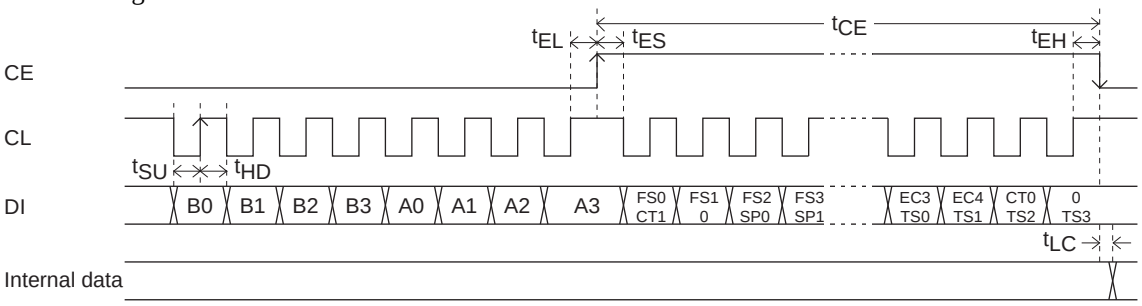
Data is input and output using the CCB (Computer Control Bus), which is Our audio IC serial bus format.
This IC adopts an 8-bit address CCB format.

	I/O mode	(LSB) Address (MSB)								Comment
		B0	B1	B2	B3	A0	A1	A2	A3	
[1]	IN1 (6A)	0	1	0	1	0	1	1	0	Control data input mode, also referred to as “ serial data input ” mode. 16bit data input mode
[2]	IN2 (6B)	1	1	0	1	0	1	1	0	

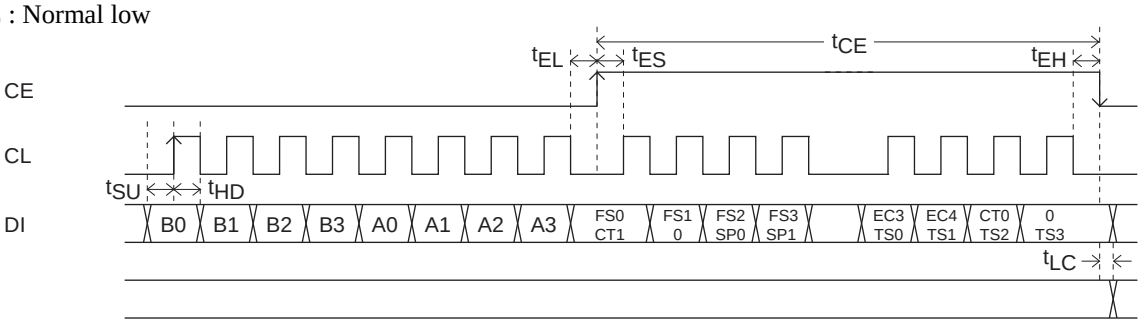
(1) Serial data input (IN1 / IN2)

t_{SU}, t_{HD}, t_{EL}, t_{ES}, t_{EH} 0.75 s t_{LC} 1.15 s t_{CE} 20 ms

CL : Normal high



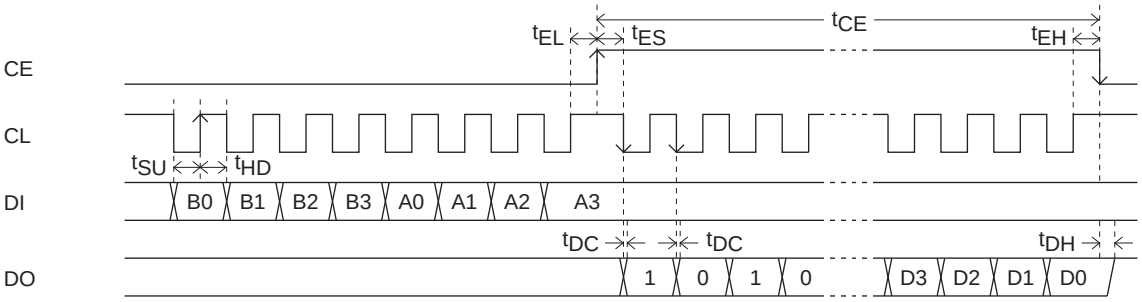
CL : Normal low



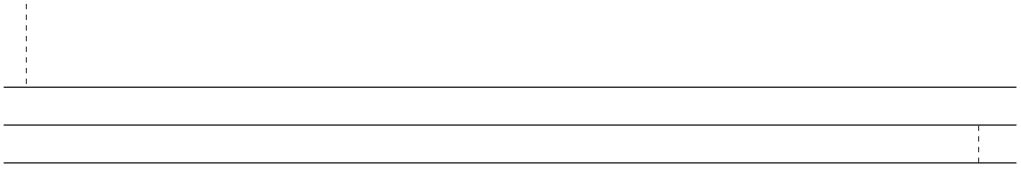
(2) Serial data output (OUT)

t_{SU}, t_{HD}, t_{EL}, t_{ES}, t_{EH} 0.75 s t_{DC}, t_{DH} 0.46 s t_{CE} 20 ms

CL : Normal high



CL : Normal low



Cautions : 1. Since the DO pin is an n-channel open-drain output, the transition times (t_{DC}, t_{DH}) will differ with the value of the pull-up resistor used.

2. The CE, CL, DI, and DO pins can be connected to the corresponding pins on other ICs that use the CCB interface. (However, we recommend connecting the DO and CE pins separately if the number of available microcontroller ports allows it.)

3. Serial data I/O becomes possible after the crystal oscillator starts oscillation.

(3) Serial data timing

CL : Normal high

CL : Normal low

Parameter	Symbol	Conditions	min	typ	max	Unit
Data setup time	t_{SU}	DI, CL	0.75			s
Data hold time	t_{HD}	DI, CL	0.75			s
Clock low level time	t_{CL}	CL	0.75			s
Clock high level time	t_{CH}	CL	0.75			s
CE wait time	t_{EL}	CE, CL	0.75			s

DO pin operation

This IC incorporates a RAM data buffer that can hold up to 24 blocks of data. At the point when one block of data is written to this RAM, the IC issues a read request by switching the DO pin from high to low.
The DO pin always goes high for a fixed period (Tdo = 265 s) after a readout and CE goes low. When all the data in the data buffer has been read out, the DO pin is held in the high state until a new block of data has been written to the RAM. If there is data that has not yet been read remaining in the data buffer, the DO pin goes low after the Tdo time has elapsed.
After a synchronization reset, the DO pin is held high until synchronization is established. It goes low at the point the IC synchronizes.

When the DO pin is high following the 265 s period (Tdo) after data is read out.
Here, the buffer is in the empty state, i.e. the state where new data has not been written. After this, when the DO pin goes low, applications are guaranteed to be able to read out that data without it being overwritten by new data if they start a readout operation within 480 ms of DO going low.

When DO goes low 265