LC72722PMS

RDS/RBDS Single-chip Signal Processor IC

ON Semiconductor®

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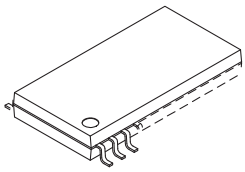

SOIC24 W / MFP24 (375 mil)

Overview

The LC72722PMS is a single-chip system IC that implement the signal processing required by the European Broadcasting Union RDS (Radio Data System) standard and by the US NRSC (National Radio System Committee) RBDS (Radio Broadcast Data System) standard. This IC include band-pass filter, demodulator, synchronization, and error correction circuits as well as data buffer RAM on chip and perform effective error correction using a soft-decision error correction technique.

Functions

Band-pass filter : switched capacitor filter (SCF)
Demodulator : RDS data clock regeneration and demodulated data reliability information
Synchronization : Block synchronization detection
(with variable backward and forward protection conditions)
Error correction : Soft-decision/hard-decision error correction
Buffer RAM : Adequate for 24 blocks of data (about 500 ms) and flag memory
Data I/O : CCB* interface (power on reset)

Features

Error correction capability improved by soft-decision error correction
The load on the control microprocessor can be reduced by storing decoded data in the on-chip data buffer RAM.
Two synchronization detection circuits provide continuous and stable detection of the synchronization.
Data can be read out starting with the backward-protection block data after a synchronization reset.
Fully adjustment free

Specifications

Operating power-supply voltage	: 4.5 to 5.5 V
Operating temperature	: 40 to +85 C
Package	: MFP24 (375 mil)

* Computer Control Bus (CCB) is an ON Semiconductor's original bus format and the bus addresses are controlled by ON Semiconductor.

ORDERING INFORMATION

See detailed ordering and shipping information on page 19 of this data sheet.

July 2017 - Rev. 1
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LC72722PMS/D

Specifications

Absolute Maximum Ratings at Ta = 25 C, Vssd = Vssa = 0 V

Parameter	Symbol	Pin Name	Ratings	Unit
Maximum supply voltage	Vddmax	Vddd, Vdda	0.3 to +7.0	V
Maximum input voltage	Vin1max	CL, DI, CE, SYR, T1, T2, T3, T4, T5, T6, T7, SYNC	0.3 to +7.0	V
	Vin2max	XIN	0.3 to Vddd+0.3	V
	Vin3max	MPXIN, CIN	0.3 to Vdda+0.3	V
Maximum output voltage	Vo1max	DO, SYNC, RDS-ID, T3, T4, T5, T6, T7	0.3 to +7.0	V
	Vo2max	XOUT	0.3 to Vddd+0.3	V
	Vo3max	FLOUT	0.3 to Vdda+0.3	V

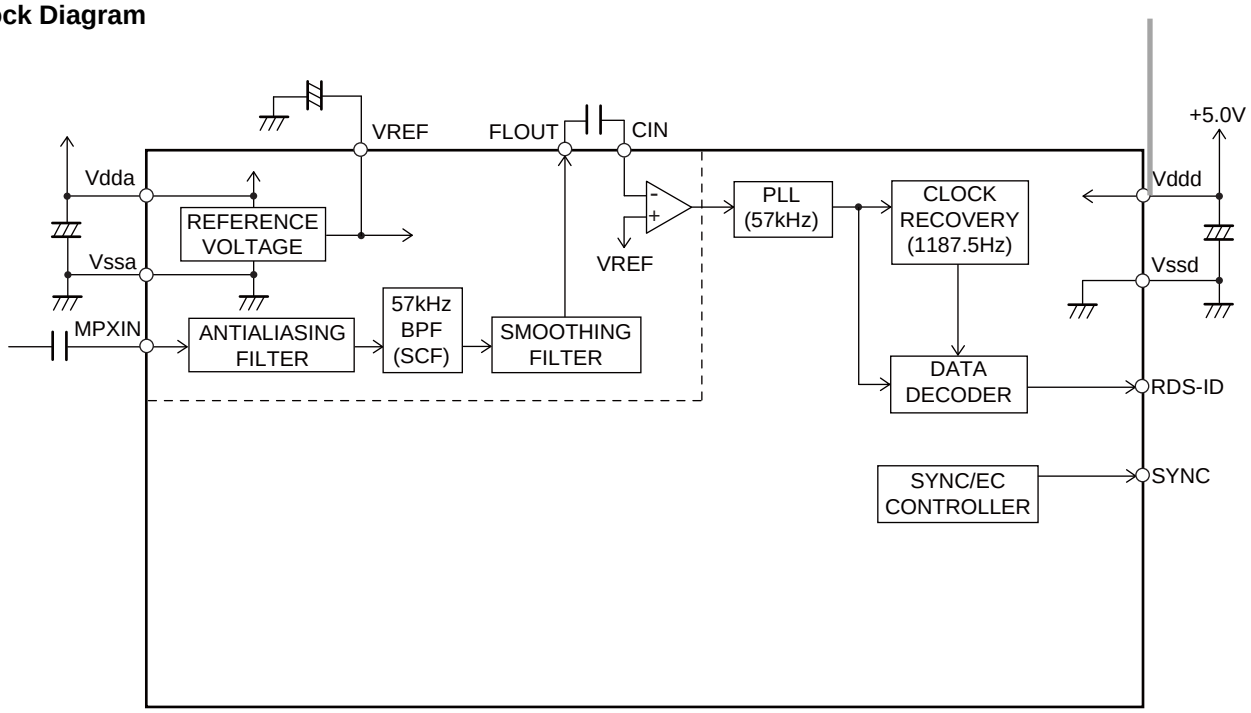
Electrical Characteristics at Ta =

Package Dimensions

unit : mm

Pin Assignment

Block Diagram



Pin Functions

Pin No.	Pin name	Function	I/O	Pin circuit
1	VREF	Reference voltage output (Vdda/2)	Output	
2	MPXIN	Baseband (multiplexed) signal input	Input	
5	FLOUT	Subcarrier output (filter output)	Output	
7	CIN	Subcarrier input (comparator input)	Input	
3	Vdda	Analog system power supply (+5 V)		
4	Vssa	Analog system ground		
12	XOUT	Crystal oscillator output (4.332 / 8.664 MHz)	Output	

ta7.02 84.72 432.3203 T34 ref384

(3) Consecutive RAM read out possible flag (1 bit) : RE

RE	RAM data information
1	The next data to be read out is in RAM
0	This data item is the last item in RAM, ant the next data is not present.

(4) RAM data remaining flag (2 bits) : RF0,RF1

RF1	RF0	Remaining data in RAM (number of blocks)
0	0	1 to 7
0	1	8 to 15
1	0	16 to 23
1	1	24

Caution : This value is only meaningful when RE is 1. When RE is 0, there is no data in RAM, even if RF is 00.
If a synchronization reset was applied using SYR, then the backward protection block data that was written to memory is also counted in this value.

(5) ARI(SK) detection flag (1bit) : ARI

ARI	SK signal
1	Detected
0	Not detected

(6) Synchronization established flag (1 bit) : SYC

SYC	Synchronization detection
1	Synchronized
0	Not synchronized

CCB Input data format

(1) Synchronization protection (forward protection) method setting (4 bits) : FS0 to FS3

Mode1 (PT2 = 0)	Pin T7 (TA)
TA = 0 detected	High (1)
TA = 1 detected	Low (0)

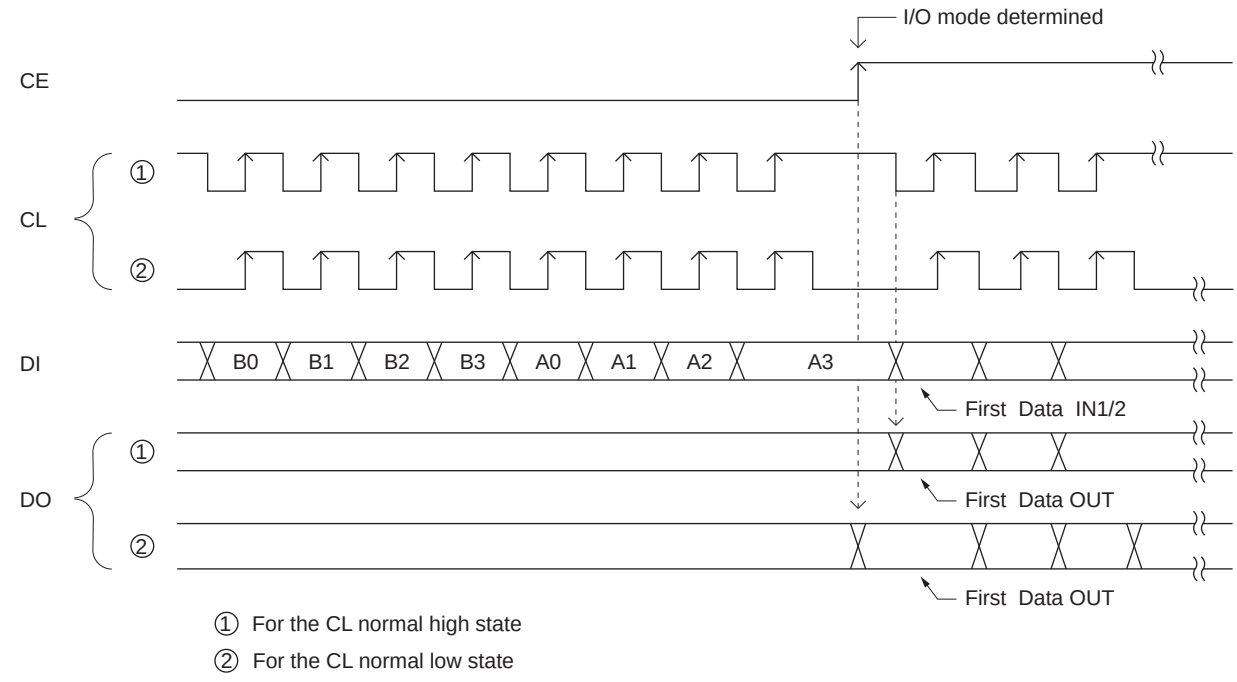
RDCL / RDDA / RSFT and ERROR / CORREC / SYNC output timing

(1) Timing 1

Serial Data Input and Output Methods

Data is input and output using the CCB (Computer Control Bus), which is Our audio IC serial bus format.
This IC adopts an 8-bit address CCB format.

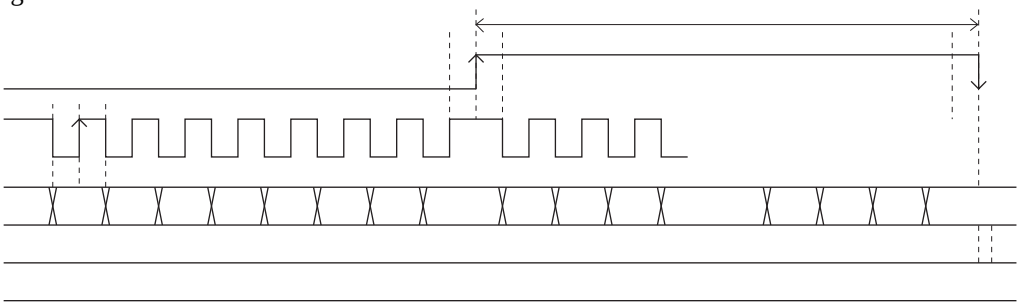
	I/O mode	(LSB) Address (MSB)								Comment
		B0	B1	B2	B3	A0	A1	A2	A3	
[1]	IN1 (6A)	0	1	0	1	0	1	1	0	Control data input mode, also referred to as " serial data input " mode. 16bit data input mode
[2]	IN2 (6B)	1	1	0	1	0	1	1	0	
[3]	OUT (6C)	0	0	1	1	0	1	1	0	Data output mode The data for multiple blocks can be output sequentially in this mode.



(1) Serial data input (IN1 / IN2)

t_{SU}, t_{HD}, t_{EL}, t_{ES}, t_{EH} 0.75 s t_{LC} 1.15 s t_{CE} 20 ms

CL : Normal high



CL : Normal low

(2) Serial data output (OUT)

t_{SU}, t_{HD}, t_{EL}, t_{ES}, t_{EH} 0.75 s t_{DC}, t_{DH} 0.46 s t_{CE} 20 ms

CL : Normal high

CL : Normal low

Cautions : 1. Since the DO pin is an n-channel open-drain output, the transition times (t_{DC}, t_{DH}) will differ with the value of the pull-up resistor used.

2. The CE, CL, DI, and DO pins can be connected to the corresponding pins on other ICs that use the CCB interface. (However, we recommend connecting the DO and CE pins separately if the number of available microcontroller ports allows it.)

3. Serial data I/O becomes possible after the crystal oscillator starts oscillation.

(3) Serial data timing

CL : Normal high

CL : Normal low

Parameter	Symbol	Conditions	min	typ	max	Unit
Data setup time	t_{SU}	DI, CL	0.75			s
Data hold time	t_{HD}	DI, CL	0.75			s
Clock low level time	t_{CL}	CL	0.75			s
Clock high level time	t_{CH}	CL	0.75			s
CE wait time	t_{EL}	CE, CL	0.75			s
CE setup time	t_{ES}	CE, CL	0.75			s
CE hold time	t_{EH}	CE, CL	0.75			s
CE high level time	t_{CE}	CE			20	ms
Data latch transition time	t_{LC}					

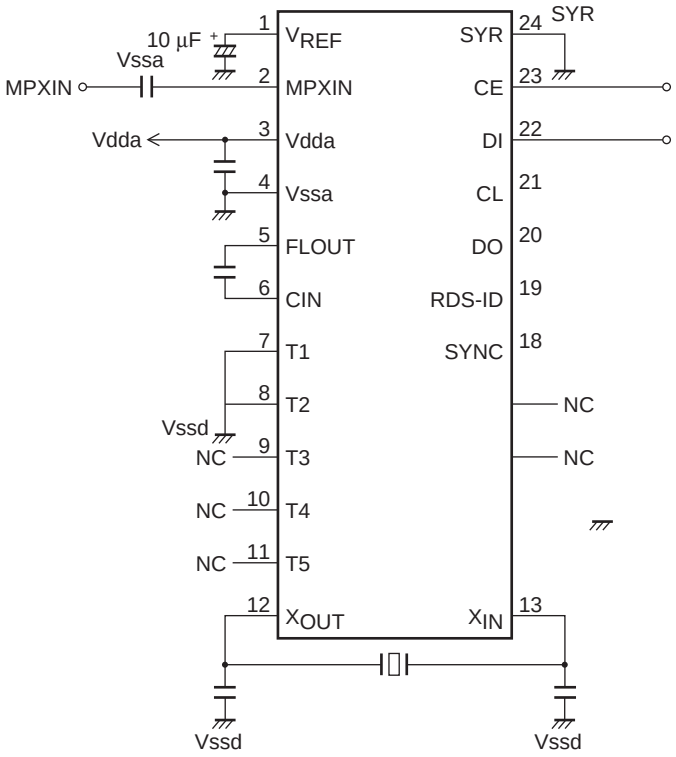
DO pin operation

This IC incorporates a RAM data buffer that can hold up to 24 blocks of data. At the point when one block of data is written to this RAM, the IC issues a read request by switching the DO pin from high to low.

The DO pin always goes high for a fixed period (Tdo = 265 s) after a readout and CE goes low. When all the data in the data buffer has been read out, the DO pin is held in the high state until a new block of data has been written to the RAM. If there is data that has not yet been read remaining in the data buffer, the DO pin goes low after the Tdo time has elapsed.

After a synchronization reset, the DO pin is held high until synchronization is established. It goes low at the point the IC synchronizes.

Sample Application circuit



Caution : 1. Determine the value of the DO pin pull-up resistor based on the required serial data transfer speed.
2. If the SYR pin is unused, it must be connected to ground.