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connected to the pins.

Functions

Volume control: 0 dB to -50 dB in 1 dB steps, -52 dB to -54 dB in 2 dB steps, and -56 dB to -58 dB in 2 dB steps, for a total of 66 positions.
A balance function can be implemented by driving the left and right channels independently.

Features

Built-in buffer amplifiers minimize the number of external components required.
Fabricated in a silicon gate CMOS process to minimize the power consumption.

LC75344MD

Allowable Operating Ranges at $T_a = 30$ to $+75$ C, $V_{SS} = 0V$

Parameter	Symbol	Pin Name	Conditions	Ratings			Unit
				min	typ	max	
Supply voltage	V_{DD}	V_{DD}		4.5		10	V
High-level input voltage	V_{IH}	CL, DI, CE		2.0		10	V
Low-level input voltage	V_{IL}	CL, DI, CE	$7.5 V_{DD} 10$	V_{SS}		0.8	V
		CL, DI, CE	$4.5 V_{DD} 7.5$	V_{SS}		0.3	V
Input voltage amplitude	V_{IN}	LIN, RIN		V_{SS}		V_{DD}	Vp-p
Input pulse width	$t_{\theta W}$	CL		1			s
Setup time	t_{setup}	CL, DI, CE		1			s
Hold time	t_{hold}	CL, DI, CE		1			s
Operating frequency	f_{opg}	CL				500	kHz

Electrical Characteristics at $T_a = 25$ C, $V_{DD} = 9V$, $V_{SS} = 0V$

Parameter	Symbol	Pin Name	Conditions	Ratings			Unit
				min	typ	max	
Input resistance	R_{in}	LIN, RIN			50		k

Overall Characteristics

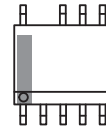
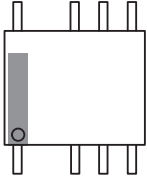
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Total harmonic distortion	THD	$V_{IN} = 1$ Vrms, $f = 1$ kHz With all settings flat overall		0.002	0.01	%
		$V_{IN} = 1$ Vrms, $f = 20$ kHz With all settings flat overall		0.003		%
Crosstalk	CT	$V_{IN} = 1$ Vrms, $f = 1$ kHz, $R_g = 1$ k With all settings flat overall	90			dB
Output noise voltage	V_N	80 kHz L.P.F, $R_g = 1$ k With all settings flat overall		6.0		V
Maximum attenuation	V_{omin}	$V_{IN} = 1$ Vrms, $f = 1$ kHz With all settings flat overall		92		dB

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Package Dimensions

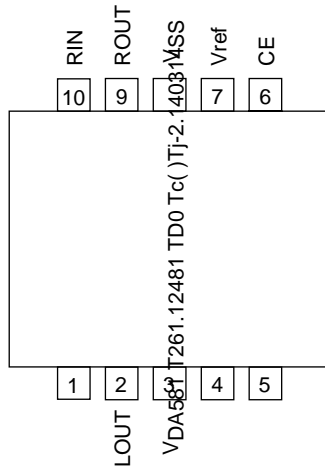
unit : mm

SOIC-10 NB
CASE 751BQ
ISSUE B



LC75344MD

Pin Arrangement

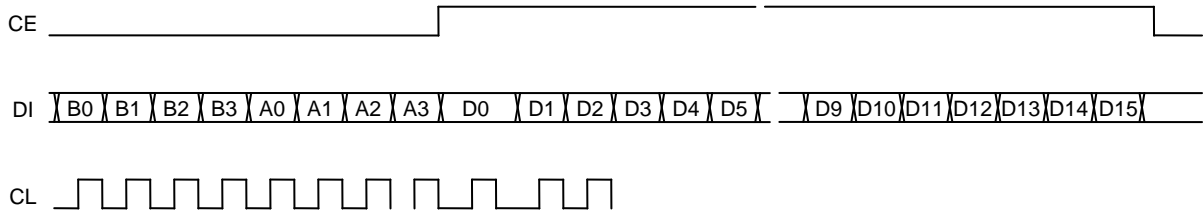


Equivalent Circuit

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Control System Timing and Data Format

The LC75344MD is controlled by inputting the stipulated data serially to the CL, DI, and CE pins. The data consists of a total of 24 bits, of which 8 bits are the address and 16 bits are the data.



Address Code (B0 to A3)

The data has an 8-bit address field, and conforms to the CCB serial bus specifications.

Address code	B0	B1	B2	B3	A0	A1	A2	A3	
(LSB)	0	0	0	1	0	0	0	1	(88HEX)

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Control Code Allocations

Volume control

D0	D1	D2	D3	D4	D5	D6	D7	Operation
0	0	0	0	0	0	0	0	0dB
1	0	0	0	0	0	0	0	1dB
0	1	0	0	0	0	0	0	2dB
1	1	0	0	0	0	0	0	3dB
0	0	1	0	0	0	0	0	4dB
1	0	1	0	0	0	0	0	5dB
0	1	1	0	0	0	0	0	6dB
1	1	1	0	0	0	0	0	7dB
0	0	0	1	0	0	0	0	8dB
1	0	0	1	0	0	0	0	9dB
0	1	0	1	0	0	0	0	10dB
1	1	0	1	0	0	0	0	11dB
0	0	1	1	0	0	0	0	12dB
1	0	1	1	0	0	0	0	13dB
0	1	1	1	0	0	0	0	14dB
1	1	1	1	0	0	0	0	15dB
0	0	0	0	1	0	0	0	16dB
1	0	0	0	1	0	0	0	17dB
0	1	0	0	1	0	0	0	18dB
1	1	0	0	1	0	0	0	19dB
0	0	1	0	1	0	0	0	20dB
1	0	1	0	1	0	0	0	21dB
0	1	1	0	1	0	0	0	22dB
1	1	1	0	1	0	0	0	23dB
0	0	0	1	1	0	0	0	24dB
1	0	0	1	1	0	0	0	25dB
0	1	0	1	1	0	0	0	26dB
1	1	0	1	1	0	0	0	27dB
0	0	1	1	1	0	0	0	28dB
1	0	1	1	1	0	0	0	29dB
0	1	1	1	1	0	0	0	30dB
1	1	1	1	1	0	0	0	31dB
0	0	0	0	0	1	0	0	32dB
1	0	0	0	0	1	0	0	33dB
0	1	0	0	0	1	0	0	34dB
1	1	0	0	0	1	0	0	35dB
0	0	1	0	0	1	0	0	36dB
1	0	1	0	0	1	0	0	37dB
0	1	1	0	0	1	0	0	38dB
1	1	1	0	0	1	0	0	39dB

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Continued from preceding page.

Volume control

























D0	D1	D2	D3	D4	D5	D6	D7	Operation
1	0	0	1	0	1	0	0	41dB
0	1	0	1	0	1	0	0	42dB
1	1	0	1	0	1	0	0	43dB
0	0	1	1	0	1	0	0	44dB
1	0	1	1	0	1	0	0	45dB
0	1	1	1	0	1	0	0	46dB
1	1	1	1	0	1	0	0	47dB
0	0	0	0	1	1	0	0	48dB
1	0	0	0	1	1	0	0	49dB
0	1	0	0	1	1	0	0	50dB
0	0	1	0	1	1	0	0	52dB
0	1	1	0	1	1	0	0	54dB
0	0	0	1	1	1	0	0	56dB
0	1	0	1	1	1	0	0	58dB
0	0	1	1	1	1	0	0	60dB
0	1	1	1	1	1	0	0	62dB
0	0	0	0	0	0	1	0	

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Pin Functions

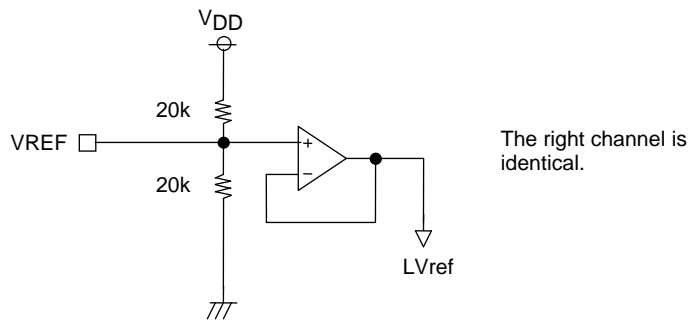
Pin name	Pin No.	Function	Notes
LIN RIN	1 10	Volume control inputs	
LOUT ROUT	2 9	Volume control outputs	
Vref	7	VDD 0.5 voltage generator block for the analog ground level. A capacitor with a value a few times 10 ⁻⁶ F must be inserted between Vref and AVSS (VSS) to minimize power supply ripple.	
VSS	8	Ground	
VDD	3	Power supply	
CE	6	Chip enable The internal latch data is written and the analog switches operate at the point this pin goes from high to low. Data transfer is enabled when this pin is at the high level.	
DI CL	4 5	Serial data and clock inputs for IC control.	

Equivalent Circuit

	LIN		
	□	0dB	
R1=5434		-1dB	R28=243
R2=4845		-2dB	R29=216
R3=4319		-3dB	R30=193
R4=3850		-4dB	R31=172
R5=3431		-5dB	R32=153
R6=3058		-6dB	R33=137
R7=2726		-7dB	R34=122
R8=2429		-8dB	R35=108
R9=2165		-9dB	R36=97
R10=1930		-10dB	R37=86
R11=1720		-11dB	R38=77
R12=1533		-12dB	R39=68
R13=1366		-13dB	R40=61
R14=1218		-14dB	R41=54
R15=1085		-15dB	R42=48
R16=967		-16dB	R43=86
R17=862		-17dB	R44=77
R18=768		-18dB	R45=69
R19=685		-19dB	R46=61
R20=610		-20dB	R47=55
R21=544		-21dB	R48=49
R22=485		-22dB	R49=87
R23=432		-23dB	R50=77
R24=385		-24dB	R51=130
R25=343		-25dB	
R26=306		-26dB	R52=104
R27=273		-27dB	

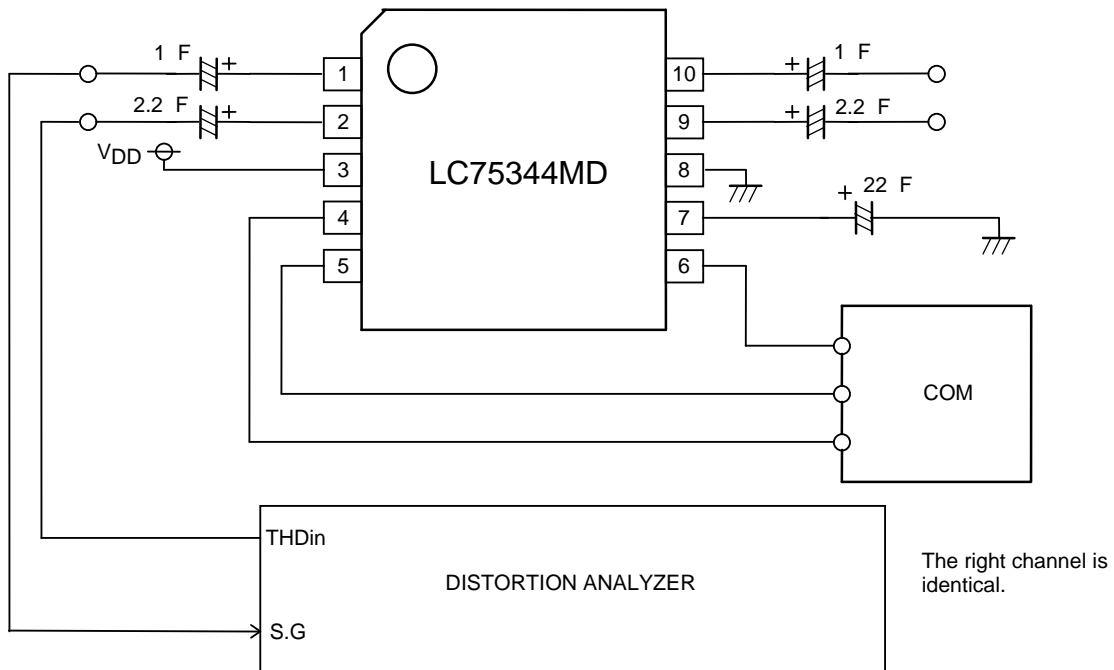
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Reference Voltage Generator Equivalent Circuit



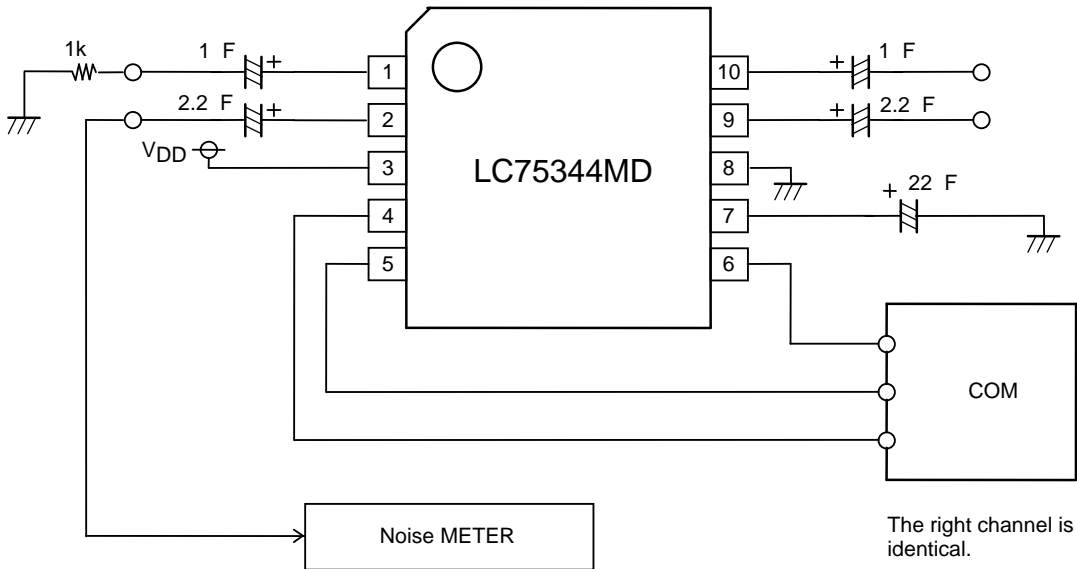
Test Circuit

Total harmonic distortion

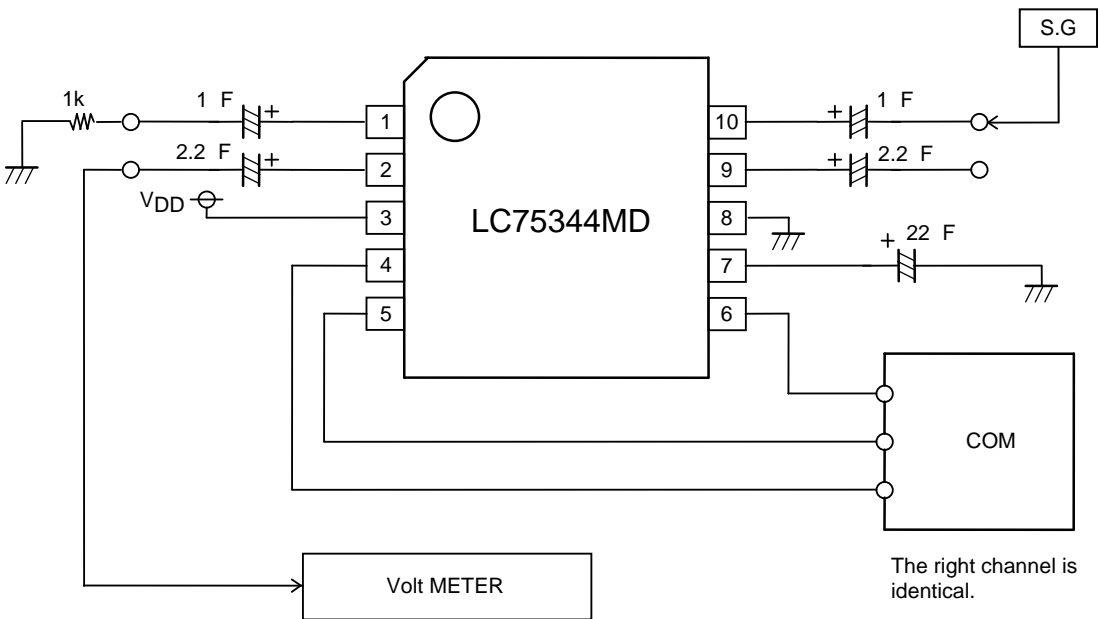


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Output noise voltage



Crosstalk

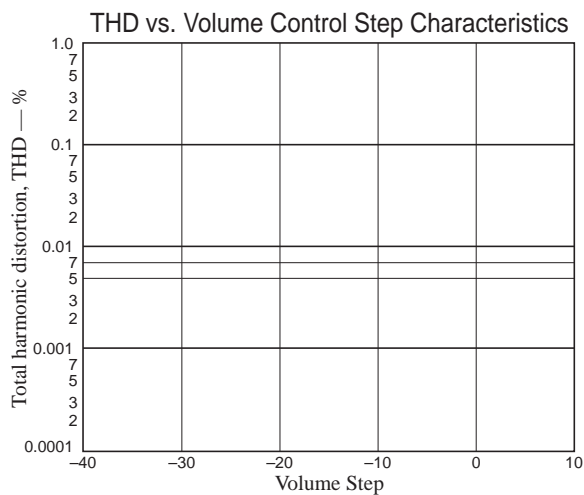
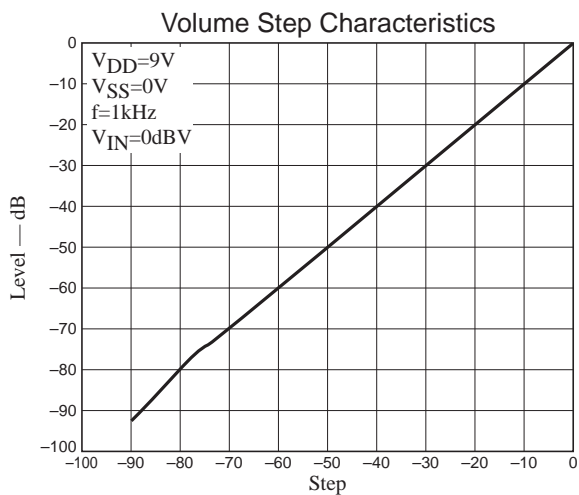


Usage Notes

The states of the internal analog switches are undefined after power is first applied. Muting must be applied externally until the control data has been sent.

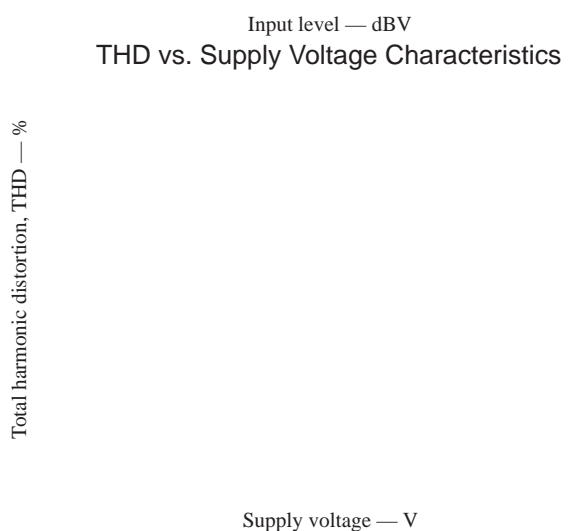
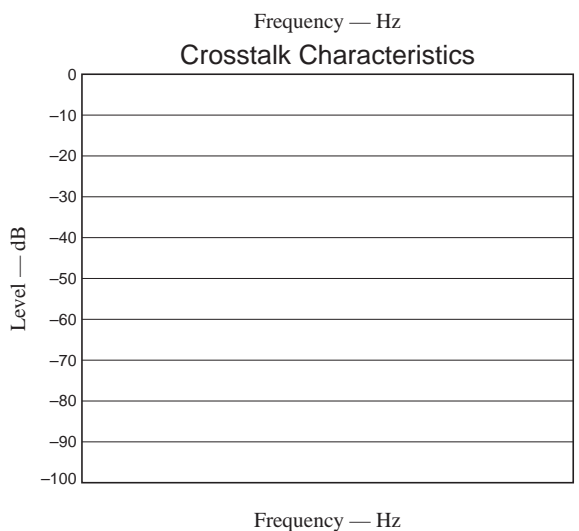
When performing the initial settings after power is first applied, both the left and right channel initial settings data must be sent before releasing the external mute.

Either cover the CL, DI, and CE lines with the ground pattern or use shielded lines to prevent high-frequency digital noise from entering the analog signal system from these lines.



THD vs. Frequency Characteristics

THD vs. Input Level Characteristics



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