rn m r b ut ns mi™, p s visit ur w bsit t
www. ns mi.c m

LC78616PE

Digital Servo Processor LSI for Compact Disc Player with RF Amplifier

ON Semiconductor®

www.onsemi.com

Overview

The LC78616PE integrates RF signal processor for CD-DA/R/RW, servo control, EFM signal processing, anti-shock processing and playback controller (Sequencer : 8bits CPU). It is possible to make CD player system using with micro controller, driver and SDRAM IC's with less components.

Features

RF signal processing for CD-DA/R/RW, servo control and EFM signal processing

Outputs CDDA, CDROM data

Maximum approximately 40 seconds shock protection by shock proof function with external 64M bits SDRAM

CD-TEXT decoded data are stored in external SDRAM.

CD playback system is realized with simple macro commands by the external controller because of the internal Sequencer (8 bits - CPU).

Op

ORDERING INFORMATION

See detailed ordering and shipping information on page 27 of this data sheet.

Detail of Functions

[CD-DSP functions]

< Playback functions>

Playback mode : CLV playback / Jitter free playback (VCEC)

Playback speed : Normal speed, double speed, quadruple speed (CLV playback / Jitter free playback)

<RF processing block>

RF system : AGC, CD-R and CD-R/W playback suppor-R/pk)

Ţ

Ţ

Ţ

Specifications

Absolute Maximum Ratings at Ta = 25°C, DV_{SS} = AV_{SS} = XV_{SS} = $VV_{SS}1$ = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	DVDD, AVDD, XVDD, VVDD1	0.3 to +3.95	V
Input voltage 1	$V_{IN}1$		0.3 to DV_{DD}+0.3	
Output voltage	V_{OUT}		0.3 to DV_{DD} +0.3	
Allowable power dissipation	Pd max	Ta ≤ 85°C Mounted reference PCB(*)	300	mW
Operating temperature	Topr		40 to +85	°C
Storage temperature	Tstg		40 to +125	

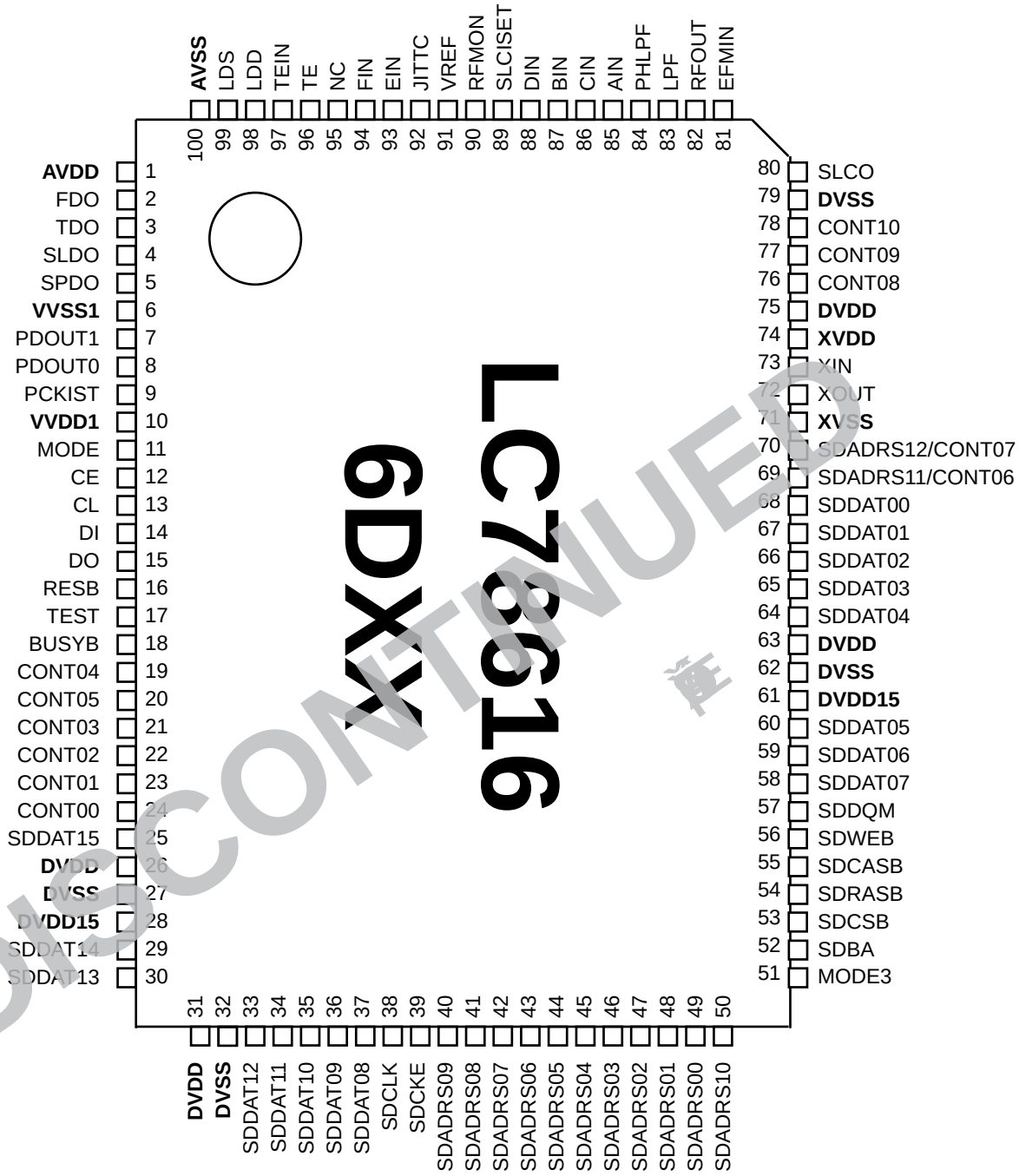
(*) Reference PCB : 114.3 mm × 76.1 mm × 1.6 mm, glass epoxy resin

<Notes>

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses a3 (mmencXD3 (mmen Tc 0.2035 Tu7 (os

LC78616PE

PIN Assignment



Pin Description

Pin No.	Pin name	I/O	State when "Reset"	Function
1	AVDD			Analog system power supply
2	FDO	AO	AVDD/2	Focus control signal output
3	TDO	AO	AVDD/2	Tracking control signal output
4	SLDO	AO	AVDD/2	Sled control signal output
5	SPDO	AO	AVDD/2	Spindle control signal output
6	VVSS1			EFMPLL ground. This pin must be connected to the 0V level.
7	PDOUT1	AO	Undefined	EFMPLL charge pump output 1
8	PDOUT0	AO	Undefined	EFMPLL charge pump output 0
9	PCKIST	AI	Input	EFMPLL charge pump current setting resistor connection pin
10	VVDD1			EFMPLL power supply
11	MODE	I	Input	LSI mode set pin. This pin must be connected to the DVDD level.
12	CE	I	Input	Host I/F Enable signal input for serial communication This pin must be connected to the

Pin No.	Pin name	I/O	State when "Reset"	Function
76	CONT08	I/O	Input	General purpose I/O port with LR clock output for CD data LR clock input for CD data (exclusive with CONT00) Data request signal input for CDTEXT interface (exclusive with CONT00 and CONT03)
77	CONT09	I/O	Input	General purpose I/O port with pull down resistor Bit clock output for CD data Bit clock input for CD data (exclusive with CONT01) Clock input/output for CDTEXT interface (exclusive with CONT01 and CONT04)
78	CONT10	I/O	Input	General purpose I/O port with pull down resistor Data output for Digital Audio interface Digital audio output<S/PDIF> Serial data output for CDTEXT interface Watch Dog Timer state monitor output
79	DVSS			Digital system ground. This pin must be connected to the 0V level.
80	SLCO	AO	Undefined	Slice Level Control output
81	EFMIN	AI	Input	RF signal input
82	RFOUT	AO	Undefined	RF signal output
83	LPF	AO	Undefined	RF signal DC level detection low-pass filter capacitor connection
84	PHLPF	AO	Undefined	Defect detection low-pass filter capacitor connection
85	AIN	AI	Input	A signal input
86	CIN	AI	Input	C signal input
87	BIN	AI	Input	B signal input
88	DIN	AI	Input	D signal input
89	SLCISET	AI	Input	SLCO output current setting resistor connection
90	RFMON	AO	Undefined	IC internal analog signal monitor
91	VREF	AO	AVDD/2	Reference voltage output for RF
92	JITTC	AO	Undefined	Jitter detection capacitor connection
93	EIN	AI	Input	E signal input
94	FIN	AI	Input	F signal input
95	NC			NC Pin (Open)
96	TE	AO	Undefined	TE signal output
97	TEIN	AI	Input	TE signal input used for TES signal generation
98	LDD	AO	Undefined	Laser power control signal output
99	LDS	AI	Input	Laser power detection signal input
100	AVSS			Analog system ground. This pin must be connected to the 0V level.

<Notes>

(1) For Unused pins :

The unused input pins must be connected to the GND(0V) level if there is no individual note in the above table.
The unused output pins must be left open(No connection) if there is no individual note in the above table.
The unused input/output pins must be connected to the GND(0V) or power supply pin for I/O block with internal pull down/up resistor OFF or be left open with internal pull down/up resistor ON when input pin mode or must be left open(No connection) when output pin mode if there is no individual note in the above table.
When you connect an I/O pin which is an input pin without internal pull-down/up resistor at reset mode to the GND or power supply level, we recommend you to use pull-down resistor or pull-up resistor individually as fail-safe.

(2) For Power supply pins :

Same voltage level must be supplied to DVDD, AVDD, XVDD and VVDD1 power supply pins.

(3) For "Reset" condition :

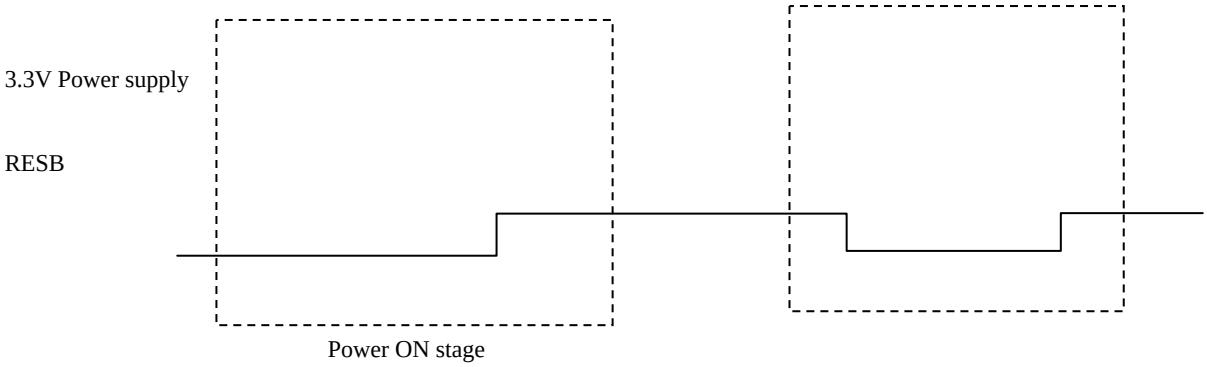
This IC is not reset only by making the RESB pin "Low".
Refer to "4. Power on and Reset control" for detail of "Reset" condition.

Power on and Reset control

Attention when power on

The RESB pin must be set to “Low” level when power is first supplied. At that time, it is necessary to input a stable clock to the XIN pin.

You may input the voltage of VDD or less to each input terminal when the power supply is off.



Parameter	Symbol	Min	Typ	Max	Unit
Reset time(Power on)	tRESW1	20			ms
Reset time(Normal) (*1)	tRESW2	1			ms

*1 : The oscillation must be stable during tRESW2.
When the XIN clock has been stopped by the command etc. , the specification of tRESW2 could be larger than the value shown above, because it takes time that the XIN oscillator becomes stable.

Command Receive Timing 1 : (Normal mode : BUSYB = "H")

*1. High level must be supplied to the DI pin during Read Access Cycle.

Command Receive Timing 2 : (Internal register open mode: BUSYB = "H")

*1. High level must be supplied to the DI pin during Read Access Cycle.

Parameter	Symbol	Pin Names	Min	Typ	Max	Unit
Setup time for READY	Trsu	CE, BUSYB	60			ns
Setup time for CE	Tcsu	CE, CL	400			
Hold time for CE	Tchd	CE, CL	200			
Setup time for DI	Twsu	DI, CL	100			
Hold time for DI	Twhd	DI, CL	100			
High level clock pulse width	Twh	CL	200			
Low level clock pulse width	Twl	CL	200			
Access time for read data	Trac	CL, DO	0		100	
Hold time for read data	Trhd	CL, DO	120			
Turn On Time for DO	Ton	CE, DO	150			
Turn Off Time for DO	Toff	CE, DO	0		300	
Command transfer time	Tce	CE	1			µs

CD data output function

Two modes can be available for CD data output.

2. Slave mode

CD Subcode Data Output function

It is possible to output the subcode data (PW data) according to the terminal setting when CD playback mode.
The PW data are output at the rising edge of SBCK signal when the SBCK clock signal is input.

<Note>
The CD-TEXT function and the CD Subcode data output function are exclusive functions. It is impossible to use those two functions simultaneously.

Used pins

SBSY (Subcode Block Synchronous signal) : CONT00
SFSY (Subcode Frame Synchronous signal) : CONT01
PW (Subcode PW data) : CONT02
SBCK (Subcode data read clock) : CONT03

Subcode Data Output timing

Subcode Block Synchronous Signal Output timing

Parameter	Symbol	Pin Names	Min	Typ	Max	unit
Subcode Read Cycle time	tSBFC	SFSY		136 *1		us

CDTEXT data output function

CDTEXT data are decoded and buffered to external SDRAM.
There are two methods to output CDTEXT data from theSDRAM.

(1) Command Communication output mode
Outputs the CDTEXT data using the command communication protocol between this IC and external host controller.

(2) Hand shake output mode using with hardware interface function
A. Inputs data request signal and transfer clock then outputs CDTEXT data
The CDTEXT data(CTDATO) will be output synchronizing with the CTCKI clock when the CTCKI clock is input after the CDTEXT data request signal is input(CTREQI = "H").
B. Inputs data request signal then outputs transfer clock and CDTEXT data
The CTCKO and CTDATO synchronized with CTCKO will be output after the CDTEXT data request signal is input (CTREQI = "H").

Internal Voltage Regulator
at Ta =

SDRAM Interface

(1) Required specification for external SDRAM

Memory size : 16M-bit or 64M-bit
Data width : 16-bit
CAS latency : 2
Burst length : Full

(2) Interface pins to external SDRAM

Pin Name	Function at 16M-bit-SDRAM	Function at 64Mbit-SDRAM	Signal name in timing chart (Page21,22)
SDDAT15 to SDDAT00	Data Input/Output (16-bit)	Data Input/Output (16-bit)	DDAT[15:0] DDAT[15:0]
SDADRS10 to SDADRS00	Address Output (11-bit)	Address Output (11-bit)	DADD[10:0] DADD[10:0]
SDADRS11	Not used *1	Address(A11) Output	DADD[11]
SDADRS12	Not used *2	Address(A12) or Bank0 Output	DADD[12]
SDBA	Bank Output	Bank or Bank1 Output	DADD[11] DADD[13]
SDDQM	DQMH/DQML (UDQM/LDQM) Output *3	DQMH/DQML (UDQM/LDQM) Output *3	SDDQM SDDQM
SDCSB	CSB Output	CSB Output	SDCSB SDCSB
SDRASB	RASB Output	RASB Output	SDRASB SDRASB
SDCASB	CASB Output	CASB Output	SDCASB SDCASB
SDWEB	WEB Output	WEB Output	SDWEB SDWEB
SDCKE	Clock Enable Output	Clock Enable Output	SDCKE SDCKE
SDCLK	Clock Output	Clock Output	SDCLK SDCLK

<Notes>

*1. SDADRS11 in 16M-bit SDRAM using mode can be used as CONT06 pin.

*2. SDADRS12 in 16M-bit SDRAM using mode can be used as CONT07 pin.

*3. The SDRAM access data width of this IC is sixteen bits. Therefore, connect the SDDQM of this IC to both the DQMH(UDQM) and DQML(LDQM) pins of SDRAM.

*4. The all pins used for SDRAM interface are input pin mode and internal pull down resistor on mode in initial condition after reset of this IC. All the resistors will be off when the SDRAM use mode is set to be ON.

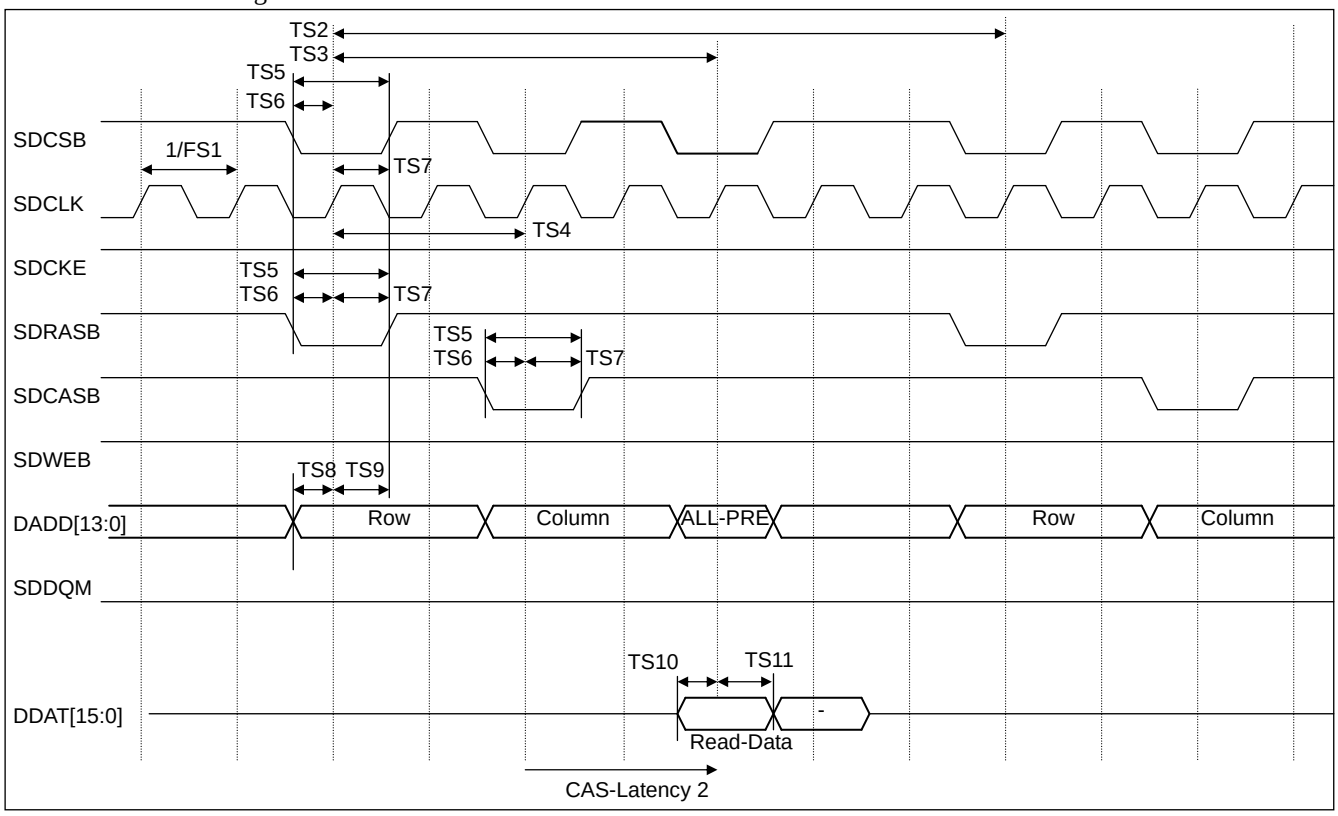
*5. Some signals used in timing chart (P21,22) use different pins according to the using SDRAM. The signal name the actual pin is shown at the most right column in above table.

Upper step : Signal name in 16Mbit-SDRAM using mode

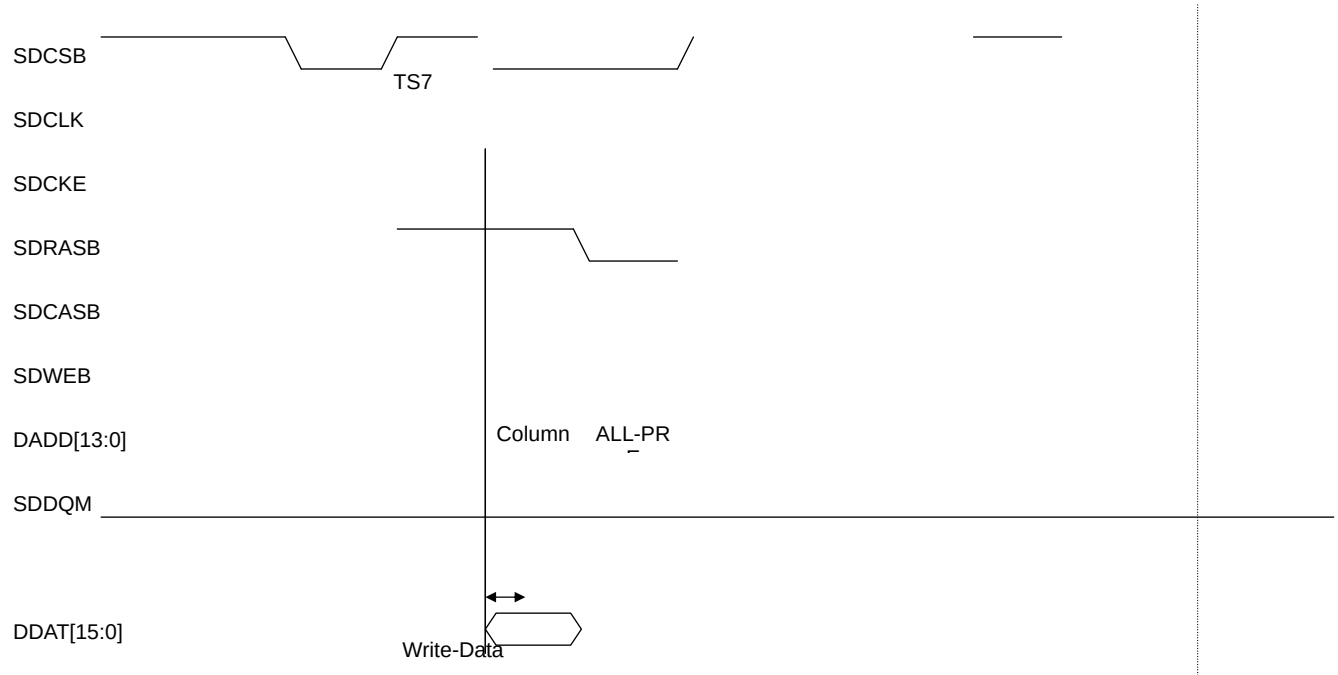
Lower step : Signal name in 64Mbit-SDRAM using mode

(3) SDRAM Access Timing

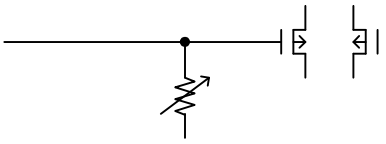
SDRAM Read Timing

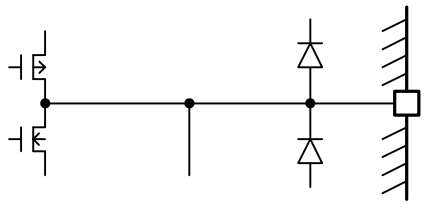
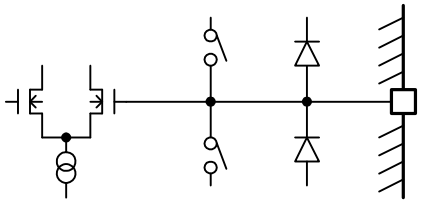
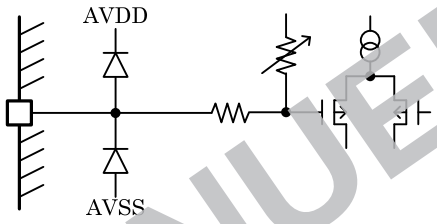
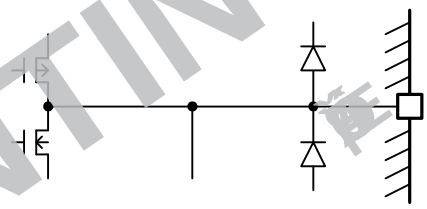
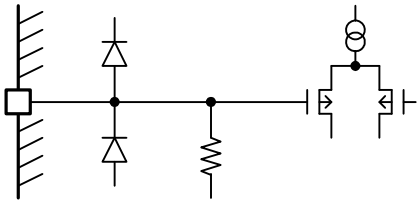
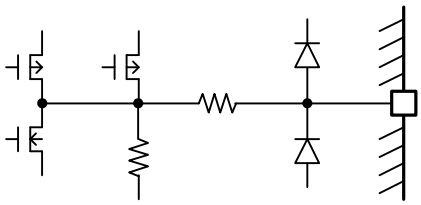
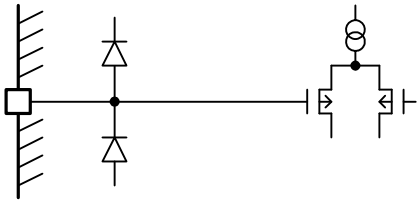


SDRAM Write Timing



Analog Pin Internal Equivalent Circuits

Pin Name (Pin No.)	Equivalent Circuit
EFMIN (81)	

Pin Name (Pin No.)	Equivalent Circuit
VREF (91)	
JITTC (92)	
EIN (93) FIN (94)	
TE (96)	
TEIN (97)	
LDD (98)	
LDS (99)	

Pin Name (Pin No.)	Equivalent Circuit
FDO (2) TDO (3) SLDO (4) SPDO (5)	

Sample Application Circuit

* This sample circuit is only for CD servo block and each PLL block.