LC87F7NP6A

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Features

LCD Driver 4COM × 54SEG
Infrared Remote Control Receiver Circuit × 2
Full duplex UART × 2

Performance

Minimum Bus Cycle Time
56ns (CF=18MHz)
Minimum Instruction Cycle Time (Tcyc)
167ns (CF=18MHz)
Operating Supply Voltage
2.7[V] to 3.6[V]
Operating Ambient Temperature
40°C to +85°C

ORDERING INFORMATION
See detailed ordering and shipping information on page 28 of this data sheet.

October 2014 - Rev. 1

Publication Order Number :
LC87F7NP6A/D

Interrupt Source Flags

31 sources, 10 vector addresses

1) Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt requests of the level equal to or lower than the current interrupt are not accepted.
2) When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address takes precedence.

No.	Vector Address	Level	Interrupt Source
1	00003H	X or L	INT0
2	0000BH	X or L	INT1
3	00013H	H or L	INT2/T0L/INT4/remote control receiver1
4	0001BH	H or L	INT3/base timer/INT5/ remote control receiver2
5	00023H	H or L	T0H/INT6
6	0002BH	H or L	T1L/T1H/INT7
7	00033H	H or L	SIO0/UART1 receive/ UART2 receive/T8L/T8H
8	0003BH	H or L	SIO1/UART1 transmit/ UART2 transmit
9	00043H	H or L	ADC/MIC/T6/T7/PWM4/PWM5
10	0004BH	H or L	Port 0/T4/T5

Priority levels X > H > L

Of interrupts of the same level, the one with the smallest vector address takes precedence.

IFLG (List of interrupt source flag function)

1) Shows a list of interrupt source flags that caused a branching to a particular vector address.

Subroutine Stack Levels

OfS -1.252 Td( )Tj/C20 1 TfT*0084>Tj/TT1 1 Tf-0.0/.4403 TC20 115..0/.4403 0 245 Td 245 Td 245w.32 495.3803

Standby Function

HALT mode: Halts instruction execution while allowing the peripheral circuits to continue operation (Some parts of the serial transfer function stop operation) .

1) Oscillation is not stopped automatically.
2) Canceled by a system reset or occurrence of an interrupt

HOLD mode: Suspends instruction execution and the operation of the peripheral circuits.

1) The CF, RC, X'tal, and multifrequency RC oscillators automatically stop operation.
2) There are three ways of resetting the HOLD mode.
   (1) Setting the reset pin to the low level
   (2) Setting at least one of the INT0, INT1, INT2, INT4, and INT5 pins to the specified level
   (3) Having an interrupt source established at port 0

X'tal HOLD mode: Suspends instruction execution and the operation of the peripheral circuits except the base timer and infrared remote controller circuit.

1) The CF, RC, and multifrequency RC oscillators automatically stop operation.
2) The state of crystal oscillation established when the X'tal HOLD mode is entered is retained.
3) There are five ways of resetting the X'tal HOLD mode.
   (1) Setting the reset pin to the low level
   (2) Setting at least one of the INT0, INT1, INT2, INT4, and INT5 pins to the specified level
   (3) Having an interrupt source established at port 0
   (4) Having an interrupt source established in the base timer circuit
   (5) Having an interrupt source established in the infrared remote control receiver circuit

On-chip Debugger Function

Supports software debugging with the IC mounted on the target board.

Package Form

QIP100E(14 20) : Pb-Free/Halogen Free type
QFP100(14 : Pb-Free/Halogen Free type [Under Development]

Development Tools

On-chip Debugger: TCB87 TypeB +LC87F7Nxx A or TCB87 TypeC (3Lines Cable) +LC87F7NxxA

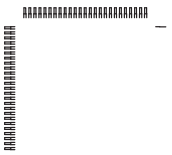
Flash ROM Programming boards

Package	Programming Boards
QIP100E(14 20)	W87FQ100

Package Dimensions

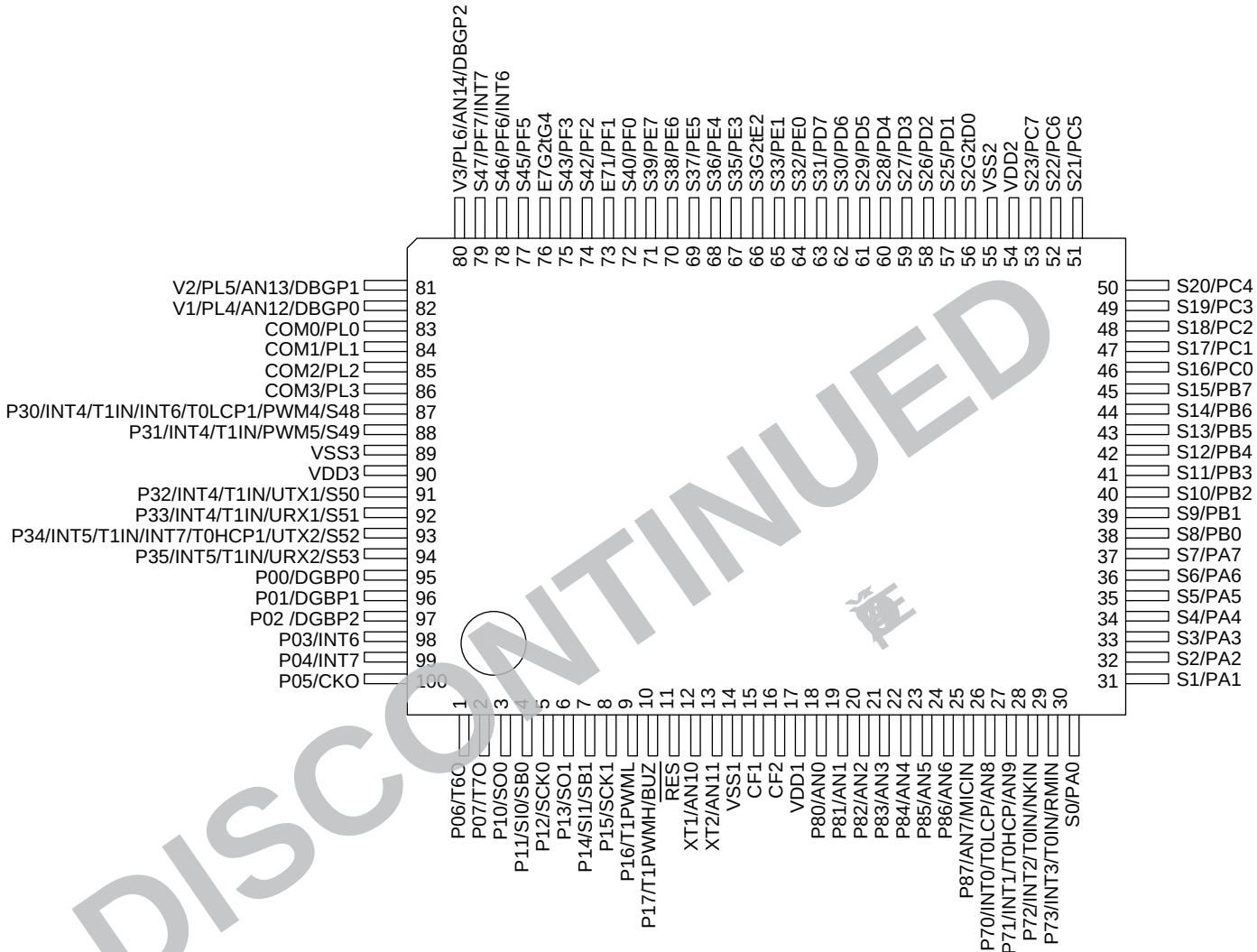
unit : mm

*Package TQFP100(14 14) type is Under Development.



Pin Assignment

QIP100E(14 20), Pb-Free/Halogen Free type



Pin Description

Pin Name	I/O	Description	Option
$V_{SS}1$ $V_{SS}2$ $V_{SS}3$	-	- power supply pin	No
$V_{DD}1$ $V_{DD}2$ $V_{DD}3$	-	+ power supply pin	No
Port 0	I/O	• 8-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistors can be turned on and off in 1-bit units. • Input for HOLD release • Input for port 0 interrupt • Shared pins P03: INT6 input P04: INT7 input P05: Clock output (system clock/can selected from sub clocB interrupt	

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Port Output Types

The table below lists the types of port outputs and the presence/absence of a pull-up resistor.
Data can be read into any input port even if it is in the output mode

Port Name	Option Selected in Units of	Option Type	Output Type	Pull-up Resistor
P00 to P07	each bit	1	CMOS	Programmable (Note)
		2	Nch-open drain	Programmable
P10 to P17	each bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P30 to P35	each bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P70	-	No	Nch-open drain	Programmable
P71 to P73	-	No	CMOS	Programmable
P80 to P87	-	No	Nch-open drain	No
S0/PA0 to S47/PF7	-	No	CMOS	Programmable
COM0/PL0 to COM3/PL3	-	No	Input only	No
V1/PL4 to V3/PL6	-	No	Input only	No
XT1	-	No	Input only	No
XT2	-	No	Output for 32.768kHz crystal oscillator (Nch-open drain when in general-purpose output mode)	No

User Option List

Option Name	Option Type	Mask Version *1	Flash Version	Option Selected in Units of	Specified Item
Port output form	P00 to P07			each bit	CMOS
					Nch-open drain
	P10 to P17			each bit	CMOS
					Nch-open drain
	P30 to P35			each bit	CMOS
					Nch-open drain
Program start address	-	*2		-	00000H
					1FF00H

*1: Mask option selection - No change possible after the mask is completed.
*2: Program start address of the mask version is 00000H.

*1: Connect the IC as shown below to minimize the noise input to the $V_{DD}1$ pin.
Be sure to electrically short the V

Allowable Operating Range at Ta = 40°C to +85°C, V_{SS}

Continued from preceding page.

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD} [V]	min	typ	max	unit
Oscillation frequency range (Note 2-3)	FmCF(1)	CF1, CF2	• 18MHz ceramic oscillation • See Fig. 1.	2.7 to 3.6		18		MHz
	FmCF(2)	CF1, CF2	• 8MHz ceramic oscillation • See Fig. 1.	2.5 to 3.6		8		
	FmRC		Internal RC oscillation	2.5 to 3.6	0.3	1.0	2.0	
	FmVMRC(1)		• Frequency variable RC source oscillation • When VMRAJ2 to 0=4, VMFAJ2 to 0=0, VMSL4M=0	2.5 to 3.6		10		
	FmVMRC(2)		• Frequency variable RC source oscillation • When VMRAJ2 to 0=4, VMFAJ2 to 0=0, VMSL4M=1	2.5 to 3.6		4		
	FsX'tal	XT1, XT2	• 32.768kHz crystal oscillation • See Fig. 2.	2.5 to 3.6		32.768		kHz
Frequency variable RC oscillation usable range	OpVMRC(1)		When VMSL4M=0	2.5 to 3.6	8	10	12	MHz
	OpVMRC(2)		When VMSL4M=1	2.5 to 3.6	3.5	4	4.5	
Frequency variable RC oscillation adjustment range	VmADJ(1)		Each step of VMRAJn (Wide range)	2.5 to 3.6	8	24	64	
	VmADJ(2)		Each step of VMFAJn (Small range)	2.5 to 3.6	1	4	8	

Note 2-3: See Tables 1 and 2 for the oscillation constants.

Continued from preceding page.

Parameter	Symbol	Pin/Remarks	Conditions

Serial I/O Characteristics at Ta = 40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3$ = 0V, 0.190εs tCYC 200εs

SIO0 Serial I/O Characteristics (Note 4-1-1) at V_{DD} = 2.7 V to 3.6V, 0.190εs tCYC 200εs

Parameter	Symbol	Pin/Remarks	Conditions	V_{DD} [V]	Specification min	typ	max	unit

SIO1 Serial I/O Characteristics (Note 4-2-1)

Parameter			Symbol	Pin/Remarks	Conditions		Specification			
						V_{DD} [V]	min	typ	max	unit
Serial clock	Input clock	Frequency	tSCK(3)	SCK1(P15)	See Fig. 6.	2.5 to 3.6	2			tCYC
		Low level pulse width	tSCKL(3)				1			
		High level pulse width	tSCKH(3)				1			
	Output clock	Frequency	tSCK(4)	SCK1(P15)	• CMOS output selected • See Fig. 6.	2.5 to 3.6	2			
		Low level pulse width	tSCKL(4)				1/2			tSCK
		High level pulse width	tSCKH(4)				1/2			
Serial input	Data setup time		tsDI(2)	SB1(P14), SI1(P14)	• Must be specified with respect to rising edge of SIOCLK. • See Fig. 6.	2.5 to 3.6	0.03			s
	Data hold time		thDI(2)			2.5 to 3.6	0.03			
Serial output	Output delay time		tdD0(4)	SO1(P13), SB1(P14)	• Must be specified with respect to falling edge of SIOCLK. • Must be specified as the time to the beginning of output state change in open drain output mode. • See Fig. 6.	2.5 to 3.6			(1/3)tCYC +0.05	

Note 4-2-1: These specifications are theoretical values. Add margin depending on its use.

Pulse Input Conditions at Ta = 40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions		Specification			
				V_{DD} [V]	min	typ	max	unit
High/low level pulse width	tPIH(1) tPIL(1)	INT0(P70), INT1(P71), INT2(P72), INT4(P30 to P33), INT5(P34 to P35), INT6(P30), INT7(P34)	• Interrupt source flag can be set. • Event inputs for timer 0 or 1 are enabled.	2.5 to 3.6	1			tCYC
	tPIH(2) tPIL(2)	INT3(P73) when noise filter time constant is 1/1	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	2.5 to 3.6	2			
	tPIH(3) tPIL(3)	INT3(P73) when noise filter time constant is 1/32	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	2.5 to 3.6	64			
	tPIH(4) tPIL(4)	INT3(P73) when noise filter time constant is 1/128	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	2.5 to 3.6	256			
	tPIH(5) tPIL(5)	MICIN(P87)	Condition that signal is accepted to small signal detection counter.	2.5 to 3.6	1			
	tPIH(6) tPIL(6)	RMIN(P73)	Condition that signal is accepted to remote control receiver circuit.	2.5 to 3.6	4			RMCK (Note 5-1)
	tPIL(7)	$\overline{RES}$						

AD Converter Characteristics at $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

<12bits AD Converter Mode at Ta = 30 to +70 C>

DD

Parameter	Symbol	Pin/Remarks	Conditions		Specification			
				V_{DD} [V]	min	typ	max	unit
Resolution	N	AN0(P80) to AN7(P87), AN8(P70), AN9(P71), AN10(XT1), AN11(XT2)		2.5 to 3.6		12		bit
Absolute accuracy	ET		(Note 6-1)	2.5 to 3.6			±16	LSB
Conversion time	tCAD		• See Conversion time calculation formulas. (Note 6-2)	3.0 to 3.6	64		115	s
				2.7 to 3.6	128		230	
				2.5 to 3.6	256		460	
Analog input voltage range	VAIN				V_{SS}		V_{DD}	V

Analog port

input cu03 Tc .rRi 3 Tm[(2.36 TT2fBT-0.000372.85.48iTT2fBTS20 1 Tf1c .rRi 6 ( )H).158TT2VrRi 6 ( )=

Consumption Current Characteristics at Ta = 40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter	Symbol	Pin/ Remarks	Conditions	V_{DD} [V]	Specification min	typ	max	unit
Normal mode consumption current (Note 7-1)	IDDOP(1)	$V_{DD}1 = V_{DD}2 = V_{DD}3$	• FmCF=18MHz ceramic oscillation mode • FmX'tal=32.768kHz crystal oscillation mode • System clock set to 12MHz side • Internal RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio	2.7 to 3.6		6.1	15.6	mA
	IDDOP(2)		• FmCF=8MHz ceramic oscillation mode • FmX'tal=32.768kHz crystal oscillation mode • System clock set to 12MHz side • Internal RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio	2.5 to 3.6		3.9	8.8	
	IDDOP(3)		• FmCF=0Hz (oscillation stopped) • FmX'tal=32.768kHz crystal oscillation mode • System clock set to internal RC oscillation • Frequency variable RC oscillation stopped. • 1/2 frequency division ratio	2.5 to 3.6		0.4	1.7	
	IDDOP(4)		• FmCF=0Hz (oscillation stopped) • FmX'tal=32.768kHz crystal oscillation mode • Internal RC oscillation stopped. • System clock set to 10MHz with frequency variable RC oscillation • 1/1 frequency division ratio	2.5 to 3.6		4.3	12.0	
	IDDOP(5)		• FmCF=0Hz (oscillation stopped) • FmX'tal=32.768kHz crystal oscillation mode • Internal RC oscillation stopped. • System clock set to 4MHz with frequency variable RC oscillation • 1/1 frequency division ratio	2.5 to 3.6		2.1	6.6	
	IDDOP(6)		• FmCF=0Hz (oscillation stopped) • FmX'tal=32.768kHz crystal oscillation mode • System clock set to 32.768kHz side • Internal RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/2 frequency division ratio	2.5 to 3.6		19.3	73	A

Note 7-1: The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors.

Continued on next page.

Continued from preceding page.

Parameter	Symbol	Pin/ Remarks	Conditions	Specification				
				V_{DD} [V]	min	typ	max	unit
HALT mode consumption current (Note 7-1)	IDDHALT(1)	$V_{DD}1$ =$V_{DD}2$ =$V_{DD}3$	• HALT mode • FmCF=18MHz ceramic oscillation mode • FmX'tal=32.768kHz crystal oscillation mode • System clock set to 12MHz side • Internal RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio	2.7 to 3.6		2.7	6.8	
	IDDHALT(2)		• HALT mode • FmCF=8MHz ceramic oscillation mode • FmX'tal=32.768kHz crystal oscillation mode • System clock set to 12MHz side • Internal RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio	2.5 to 3.6		1.4	3.1	
	IDDHALT(3)		• HALT mode • FmCF=0Hz (oscillation stopped) • FmX'tal=32.768kHz crystal oscillation mode • System clock set to internal RC oscillation • Frequency variable RC oscillation stopped. • 1/2 frequency division ratio	2.5 to 3.6		0.2	0.75	mA
	IDDHALT(4)		• HALT mode • FmCF=0Hz (oscillation stopped) • FmX'tal=32.768kHz crystal oscillation mode • Internal RC oscillation stopped. • System clock set to 10MHz with frequency variable RC oscillation • 1/1 frequency division ratio	2.5 to 3.6		1.6	4.6	
	IDDHALT(5)		• HALT mode • FmCF=0Hz (oscillation stopped) • FmX'tal=32.768kHz crystal oscillation mode • Internal RC oscillation stopped. • System clock set to 4MHz with frequency variable RC oscillation • 1/1 frequency division ratio	2.5 to 3.6		0.7 reef40 -1.S.) \8	1.75	t a

F-ROM Write Characteristics at Ta = +10°C to +55°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

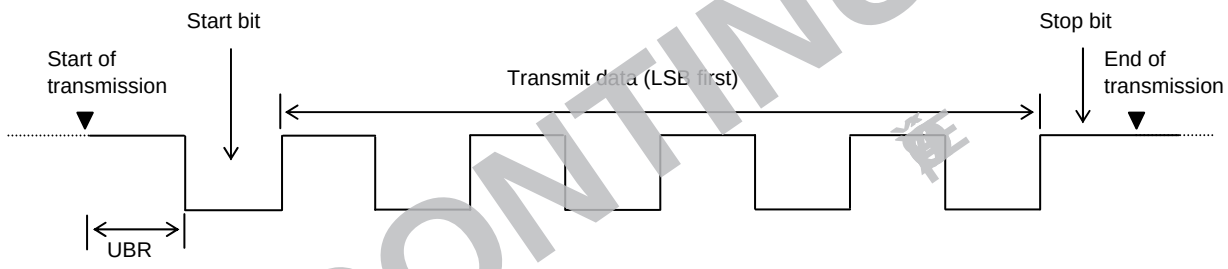
Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD} [V]	min	typ	max	unit
Onboard programming current	IDDFW(1)	$V_{DD}1$	• Without CPU current	3.0 to 3.6		7	11	mA
Programming time	tFW(1)		• 2K-byte erase operation	3.0 to 3.6		12	15	ms
	tFW(2)		• 2K-byte writing operation	3.0 to 3.6		35	45	s

UART (Full Duplex) Operating Conditions at Ta = +40 to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

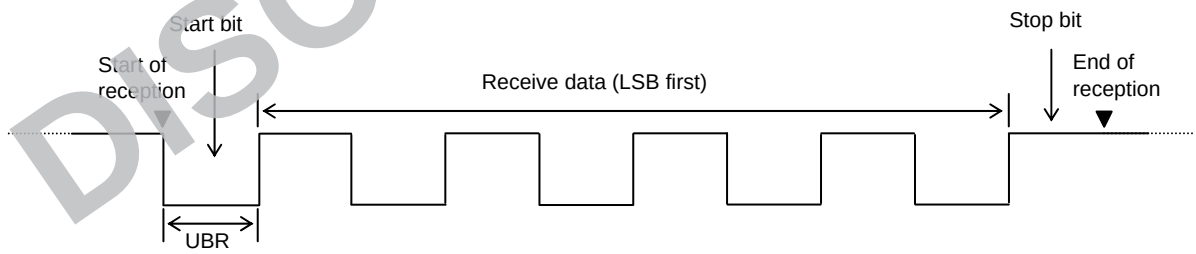
Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD} [V]	min	typ	max	unit
Transfer rate	UBR	UTX(S32), URX(S33)		2.5 to 3.6	16/3		8192/3	tCYC

Data length: 7/8/9 bits (LSB first)
Stop bits: 1 bit (2-bit in continuous data transmission)
Parity bits: None

Example of 8-bit Data Transmission Mode Processing (Transmit Data=55H)



Example of 8-bit Data Reception Mode Processing (Receive Data=55H)



Characteristics of a Sample Main System Clock Oscillation Circuit

Given below are the characteristics of a sample main system clock oscillation circuit that are measured using a Our designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 1 Characteristics of a Sample Main System Clock Oscillator Circuit with a Ceramic Oscillator

Nominal Frequency	Vendor Name	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C1 [pF]	C2 [pF]	Rf1 [ ]	Rd1 [ ]		typ [ms]	max [ms]	
18MHz	MURATA	CSTCE18M0V51-R0	(5)	(5)	OPEN	150	2.7 to 3.6	0.05	0.15	Values shown in parentheses are capacitance included in the oscillator
		CSTLS18M0X51-B0	(5)	(5)	OPEN	0	2.7 to 3.6	0.11	0.33	
10MHz	MURATA	CSTCE10M00G52-R0	(10)	(10)	OPEN	680	2.5 to 3.6	0.05	0.15	Values shown in parentheses are capacitance included in the oscillator
		CSTLS10M00G53-B0	(15)	(15)	OPEN	1.5k	2.5 to 3.6	0.05	0.15	
8MHz	MURATA	CSTCE8M00G52-R0	(10)	(10)	OPEN	680	2.5 to 3.6	0.05	0.15	Values shown in parentheses are capacitance included in the oscillator
		CSTLS8M00G53-B0	(15)	(15)	OPEN	1.5k	2.5 to 3.6	0.05	0.15	

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after V_{DD} goes above the operating voltage lower limit (see Figure 4).

Characteristics of a Sample Subsystem Clock Oscillator Circuit

Given below are the characteristics of a sample subsystem clock oscillation circuit that are measured using a Our designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 2 Characteristics of a Sample Subsystem Clock Oscillation Circuit with a Crystal Oscillation

Nominal Frequency	Vendor Name	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C3 [pF]	C4 [pF]	Rf2 [ ]	Rd2 [ ]		typ [s]	max [s]	
32.768kHz	EPSON TOYOCOM	MC-306	9	9	Open	330k	2.5 to 3.6	1.0	3.0	CL=7.0pF

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after the instruction for starting the subclock oscillation circuit is executed and to the time interval that is required for the oscillation to get stabilized after the HOLD mode is reset (see Fig. 4).

Caution: The components that are involved in oscillation should be placed as close to the IC and to one another as possible because they are vulnerable to the influences of the circuit pattern.

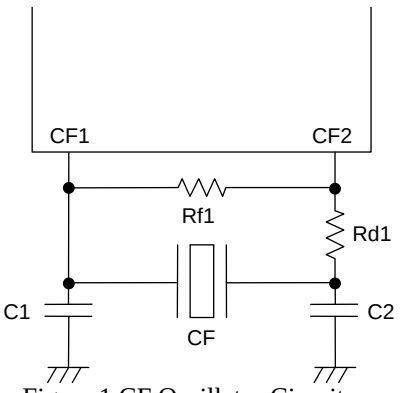


Figure 1 CF Oscillator Circuit

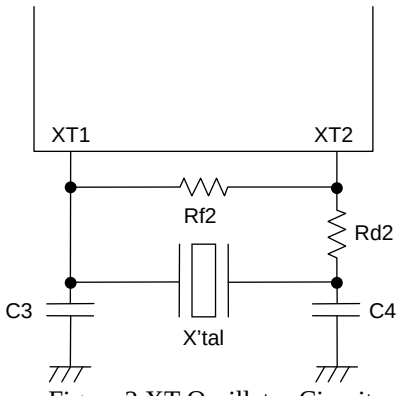


Figure 2 XT Oscillator Circuit

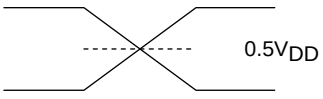
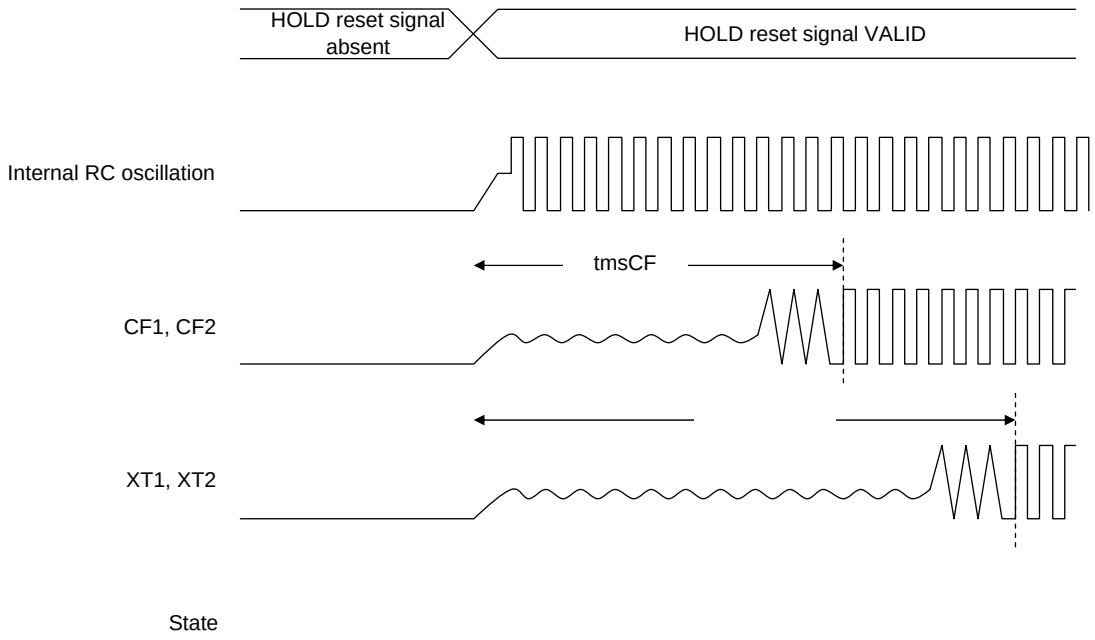


Figure 3 AC Timing Measurement Point

Reset Time and Oscillation Stabilization Time



HOLD Reset Signal and Oscillation Stabilization Time

Figure 4 Oscillation Stabilization Times

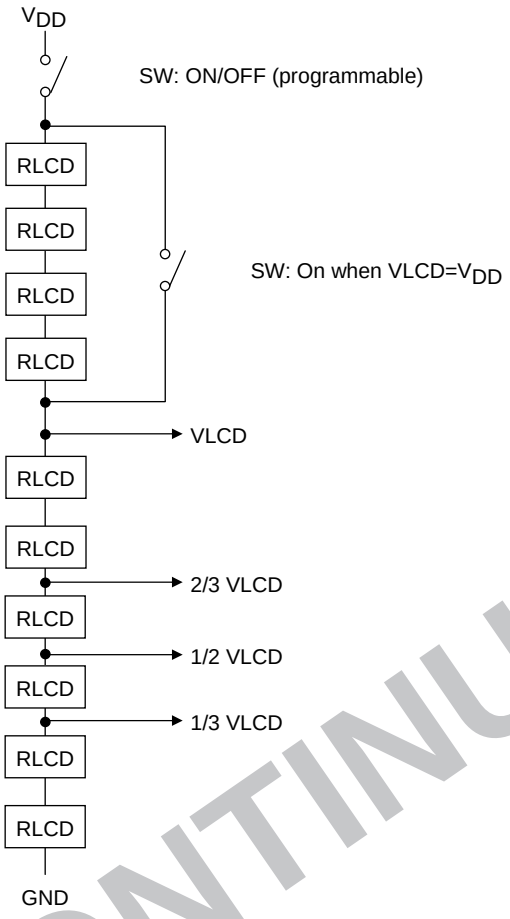


Figure 8 LCD bias resistor

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LC87F7NC8AUEJ-2H	QIP100E(14 20) (Pb-Free / Halogen Free)	50 / Tray Foam
LC87F7NC8AVUEJ-2H	QIP100E(14 20) (Pb-Free / Halogen Free)	50 / Tray Foam