Serial Flash Memory
16 Mb (2048K x 8)
LE25S161

Overview

–

– –

Features•

PACKAGE TYPES AND PIN CONFIGURATIONS

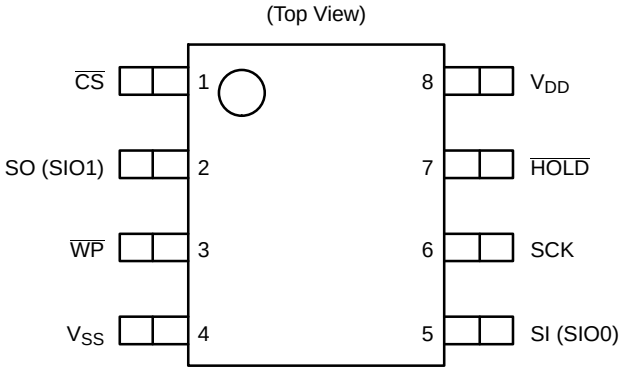


Figure 1. SOIC8 (LE25S161MDTWG) and VSOIC8 NB (LE25S161FDTWG)

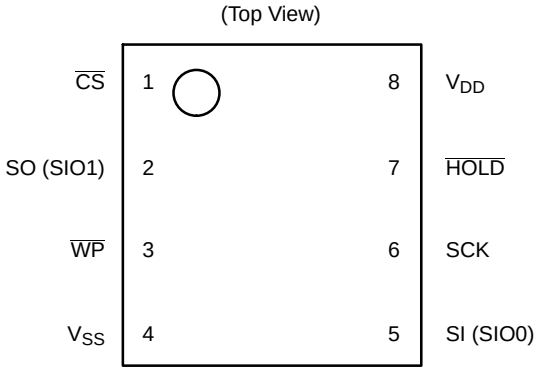


Figure 2. UDFN8 (LE25S161PCTXG)

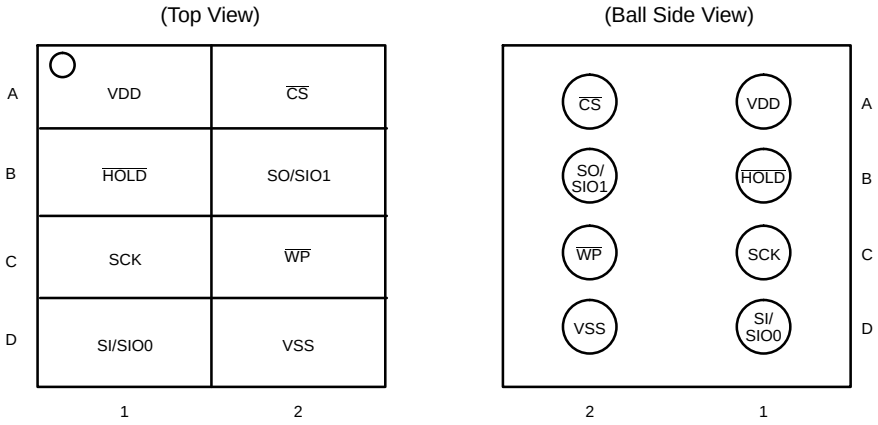


Figure 3. WLCSP8 (LE25S161XBTAG)

Table 1. PIN CONFIGURATION

Pad No.	Name
A2	$\overline{CS}$
B2	SO (SIO1)
C2	$\overline{WP}$
D2	V_{SS}
D1	SI (SIO0)
C1	SCK
B1	$\overline{HOLD}$
A1	V_{DD}

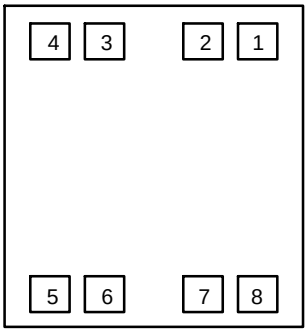


Figure 4. KGD

Table 2. PIN CONFIGURATION

Pad No.	Name
1	$\overline{CS}$
2	SO (SIO1)
3	$\overline{WP}$
4	V_{SS}
5	SI (SIO0)
6	SCK
7	$\overline{HOLD}$
8	V_{DD}

PIN DESCRIPTION

Table 3. PIN DESCRIPTION

Symbol	Pin Name	IIO	Description
$\overline{CS}$	Chip Select	I	The device becomes active when the logic level of this pin is low; it is deselected and placed in standby status when the logic level of the pin is high.
SCK	Serial Clock	I	This pin controls the data input/output timing. The input data and addresses are latched synchronized to the rising edge of the serial clock, and the data is output synchronized to the falling edge of the serial clock.
SI (SIO0)	Serial Data Input (Serial Data Input Output) timing. The input data and a220 8 123It chang1 Tinto.9071 refBT4.43durjT*Tc Due lopera re.Tc(Seria(clock.)BT8 0 0 8 76.6488 241.852g edge oBT8 0		

BLOCK DIAGRAM

Figure 5. Block Diagram

DEVICE OPERATION

Standard SPI Modes

Figure 6. SPI Modes

Table 5. Command Settings

(Standard SPI)

Table 5. COMMAND SETTINGS (STANDARD SPI) − MAX: 70 MHz (EXCEPT RDLP)

Command	Description (Clock Number)	1st Byte (0−7)	2nd Byte (8−15)	3rd Byte (16−23)	4th Byte (24−31)	5th Byte (32−39)	6th Byte (40−47)	Nth Byte (8N−8 to 8N−1)
WREN	Write Enable	06h						
WRDI	Write Disable	04h						
RDSR	Read Status Register	05h						
WRSR	Write Status Register	01h	DATA					
RDLP	-07.603 635.811 .90709 15.3:5 Byte	Tm(Description)Tj-.9709 -1.2331 TD-.0007 Tc-.0005 Tw[((Clock)8o96.31.846 .90709 15.364 ref15.3:5						Tm(Des

MEMORY ORGANIZATION

Table 7. MEMORY ORGANIZATION (16 Mbits)

Sector (64 kB) Symbol: SE	Small Sector (4 kB) Symbol: SSE	Address Space (A23 to A0)	
31	SSE[511]	1FF000h	1FFFFFh
	to		
	SSE[496]	1F0000h	1F0FFFh
30 to 6	SSE[495]	1EF000h	1EFFFFh
	to		
	SSE[96]	060000h	060FFFh
5	SSE[95]	05F000h	05FFFFh
	to		
	SSE[80]	050000h	050FFFh
4	SSE[79]	04F000h	04FFFFh
	to		
	SSE[64]	040000h	040FFFh
3	SSE[63]	03F000h	03FFFFh
	to		
	SSE[48]	030000h	030FFFh
2	SSE[47]	02F000h	02FFFFh
	to		
	SSE[32]	020000h	020FFFh
1	SSE[31]	01F000h	01FFFFh
	to		
	SSE[16]	010000h	010FFFh
0	SSE[15]	00F000h	00FFFFh
	to		
	SSE[4]	004000h	004FFFh
	SSE[3]	003800h	003FFFh
		003000h	0037FFh
	SSE[2]	002800h	002FFFh
		002000h	0027FFh
	SSE[1]	001800h	001FFFh
		001000h	0017FFh
	SSE[0]	000800h	000FFFh
		000000h	0007FFh

STATUS REGISTERS

Table 8. Status registers

Table 8. STATUS REGISTERS

Bit	Name	Logic	Function	Power−on Time Information
Bit0	$\overline{\text{RDY}}$	0	Ready	3
		1	Erase/Program	
Bit1	WEN	0	Write disabled	0
		1	Write enabled	
Bit2	BP0	0	Block protect information Protected area switch	Nonvolatile information
		1		
Bit3	BP1	0		
		1		
Bit4	BP2	0		
		1		
Bit5	TB	0	Block protect Upper side/Lower side switch	Nonvolatile information
		1		
Bit6	SUS	0	Erase/Program is not suspended	0
		1	Erase/Program suspended	
Bit7	SRWP	0	Write Status Register enabled	Nonvolatile information
		1	Write Status Register disabled	

13. All non−volatile bits of the status registers−1 are set “0” in the factory.

Contents of Each Status Register

$\overline{\text{RDY}}$ (Bit 0)

-
-

WEN (Bit 1)

–

- –
-

Table 9. PROTECTION LEVEL SETTING CONDITIONS

Protected Level	Protected Block	Status Register Bits				Protected Area
		TB	BP2	BP1	BP0	
0	Whole area unprotected	X	0	0	0	None
T1	Upper side 1/32 protected	0	0	0	1	1F0000h to 1FFFFFh
T2	Upper side 1/16 protected	0	0	1	0	1E0000h to 1FFFFFh
T3	Upper side 1/8 protected	0	0	1	1	1C0000h to 1FFFFFh
T4	Upper side 1/4 protected	0	1	0	0	180000h to 1FFFFFh
T5	Upper side 1/2 protected	0	1	0	1	100000h to 1FFFFFh
B1	Lower side 1/32 protected	1	0	0	1	000000h to 00FFFFh
B2	Lower side 1/16 protected	1	0	1	0	000000h to 01FFFFh
B3	Lower side 1/8 protected	1	0	1	1	000000h to 03FFFFh
B4	Lower side 1/4 protected	1	1	0	0	000000h to 07FFFFh
B5	Lower side 1/2 protected	1	1	0	1	000000h to 0FFFFFh
6	Whole area protected	X	1	1	X	000000h to 1FFFFFh

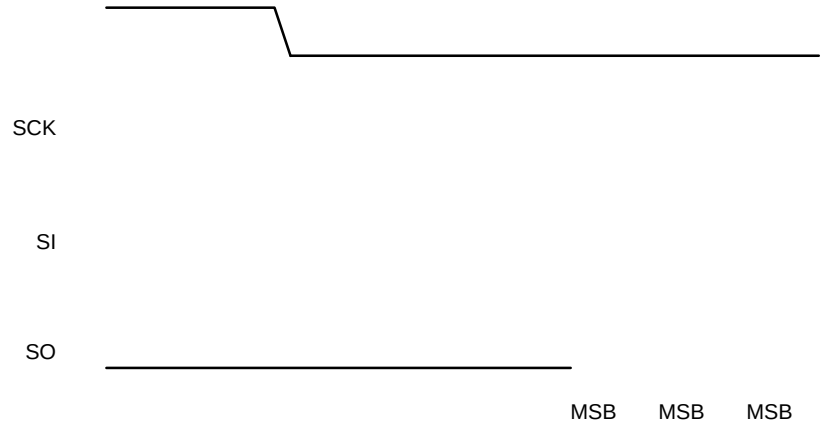
14. Chip Erase is enabled only when the protection level is 0.

DESCRIPTION OF COMMANDS AND OPERATIONS

Read Status Register (RDSR)

-
-
-

Figure 7. Read Status Register (RDSR)



- DATA: Status Resister, “*Table 8. Status Register*”

Figure 7. Read Status Register (RDSR)

Write Status Register (WRSR)

Figure 8. Write Status Register (WRSR)

Figure 37. Write Status Register Flowcharts

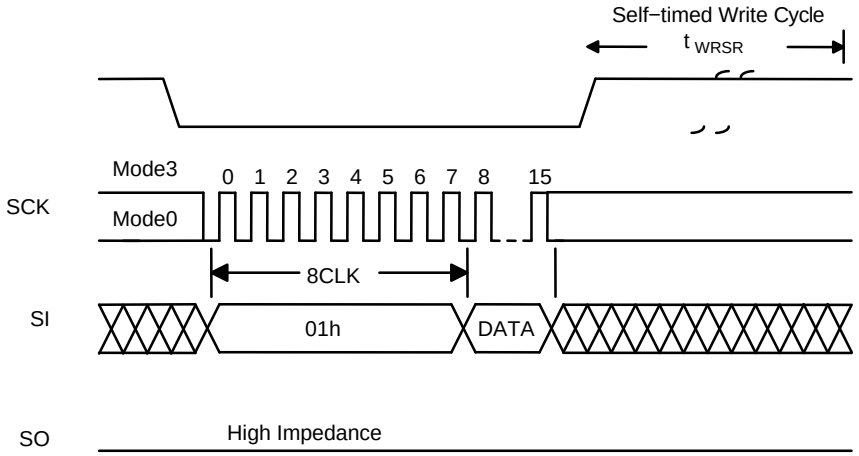
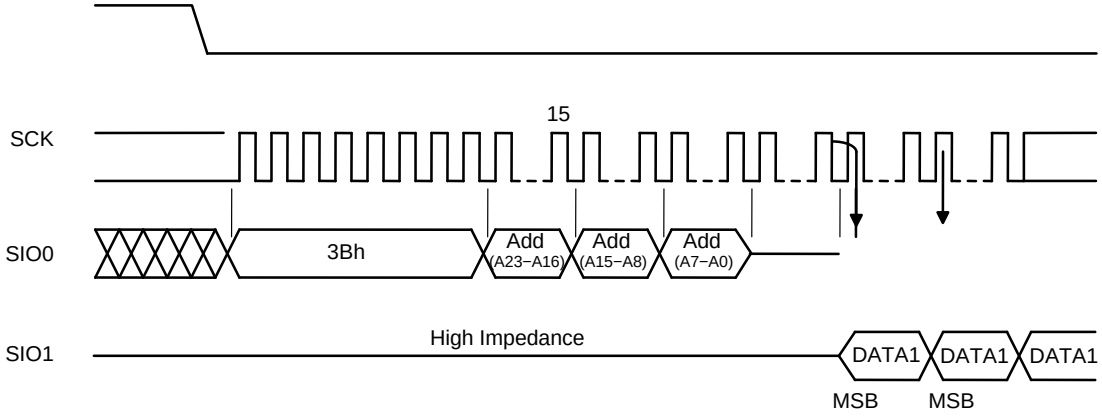


Figure 8. Write Status Register (WRSR)

High Speed Read Command (RDHS) Maximum Clock frequency: 70 MHz

Figure 12. High Speed Read (RDHS)

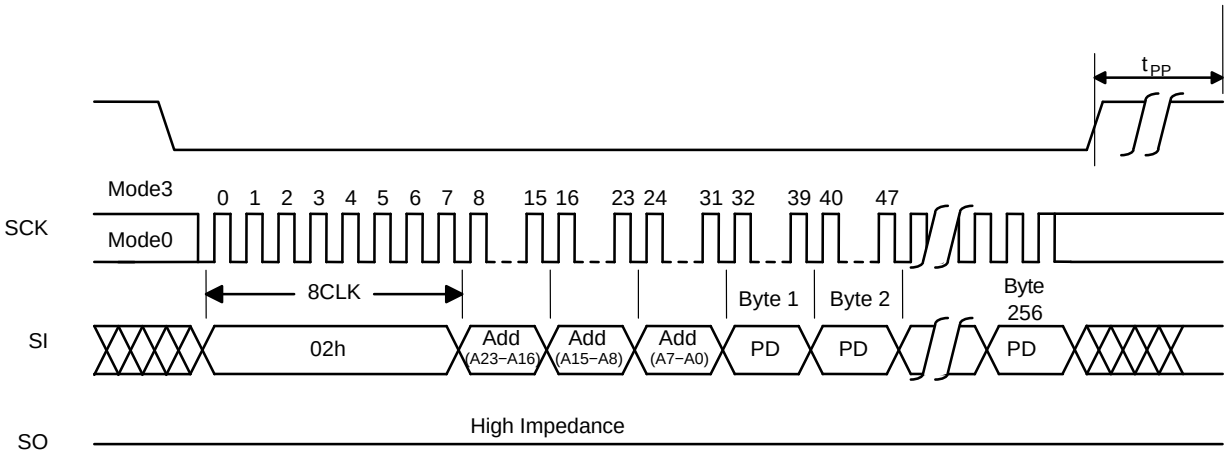


- Address A23 to A21 are “Don’t care”.

DATA0: bit6, bit4, bit2, bit0
DATA1: dit7, bit5, bit3, bit1

Figure 13. Dual Output Read (RDDO)

LE25S161



- Address A23 to A21, A15 to A0 are “Don’t care”.

Figure 18. Normal Page Program (PP)

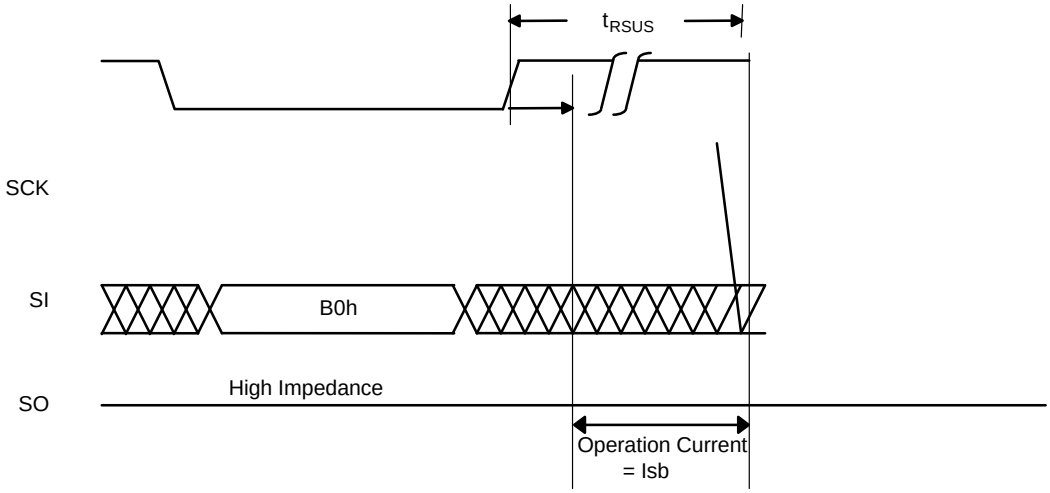


Figure 20. Write Suspend (WSUS)

Table 12. JEDEC ID CODES

		Output Code
Manufacturer code		62h
2 byte device ID	Memory type	16h
	Memory capacity code	15h (16 MBit)
Reserve code		00h

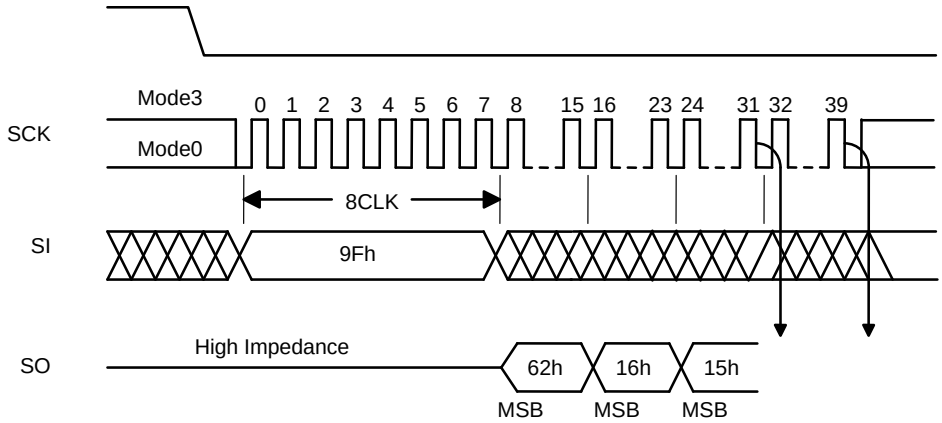


Figure 22. Read JEDEC ID (RJID)

Read Device ID (RDDI)

Table 13. Device ID Code
Figure 26. Read Device ID

Figure 26. Read Device ID

Read SFDP (RSFDP)

Table 14. SFDP Header
Table 15. SFDP Parameter Table

Figure 28. Read SFDP (RSFDP)

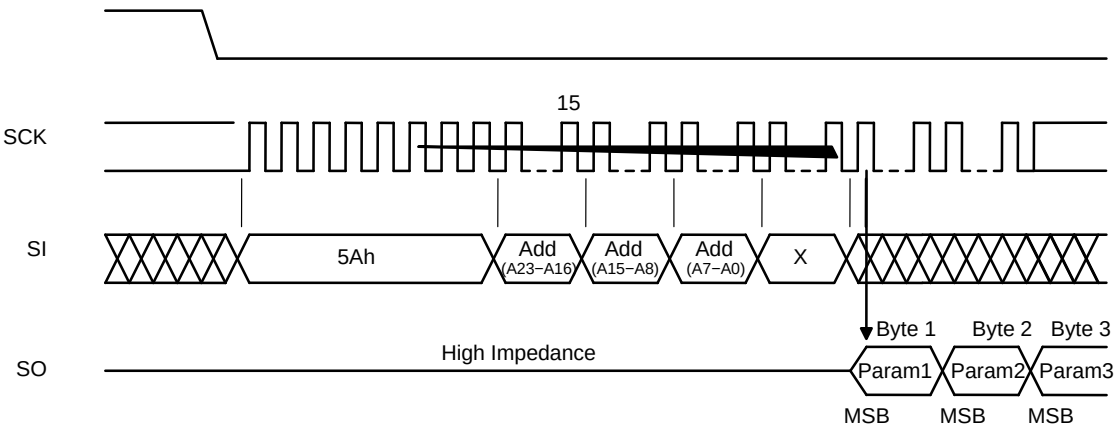


Figure 28. Read SFDP (RSFDP)

Table 15. SFDP PARAMETER TABLE

Description	Comment	Byte

Table 15. SFDP PARAMETER TABLE (continued)

Description	Comment	Byte Address (Hex)	Bits	Data (Binary)	Data (Hex)
JDEC BASIC FLASH PARAMETER TABLES (FROM 5th DWORD TO 8th DWORD)					
(2−2−2) Fast Read	0 = not support 1 = support	50h	0	0b	EEh
Reserved	Default all 1's		3:1	111b	
(4−4−4) Fast Read	0 = not support 1 = support		4	0b	
Reserved	Default all 1's		7:5	111b	
Reserved	Default all 1's	51h 52h 53h	31:8	−	FFh FFh FFh
Reserved	Default all 1's	54h 55h	15:0	−	FFh FFh
(2−2−2) Fast Read Number of Wait states (Dummy Clocks)	0 0000b: Wait states (dummy Clocks) not support	56h	20:16	0_0000b	00h
(2−2−2) Fast Read Number of Mode Clocks	000b: Mode Bits not support		23:21	000b	
(2−2−2) Fast Read Instruction		57h	31:24	1111_1111b	FFh
Reserved	Default all 1's	58h 59h	15:0	−	FFh FFh
(4−4−4) Fast Read Number of Wait States (Dummy Clocks)	0 0000b: Wait states (dummy Clocks) not support	5Ah	20:16	0_0000b	00h
(4−4−4) Fast Read Number of Mode Clocks	000b: Mode Bits not support		23:21	000b	
(4−4−4) Fast Read Instruction		5Bh	31:24	1111_1111b	FFh
Sector Type 1 Size	Sector/block size = 2^N bytes 0Ch indicates 4 kbytes	5Ch	7:0	0000_1100b	0Ch
Sector Type 1 Erase Instruction		5Dh	15:8	0010_0000b	20h
Sector Type 2 Size	Sector/block size = 2^N bytes 10h indicates 64 kbytes	5Eh	23:16	0001_0000b	10h
Sector Type 2 Erase Instruction		5Fh	31:24	1101_1000b	D8h
JDEC BASIC FLASH PARAMETER TABLES (FROM 9th DWORD TO 12th DWORD)					
Sector Type 3 Size	Sector/block size = 2^N bytes 00h indicates not exist	60h	7:0	0000_0000b	00h
Sector Type 3 Erase Instruction		61h	15:8	1111_1111b	FFh
Sector Type 4 Size	Sector/block size = 2^N bytes 00h indicates not exist	62h	23:16	0000_0000b	00h
Sector Type 4 Erase Instruction		63h	31:24	1111_1111b	FFh
Multiplier from Typical Erase Time to Maximum Erase Time	SE (64 k−Byte erase): 150 ms = 2 x (n + 1) x 15 ms n = 4	64h	3:0		

Table 15. SFDP PARAMETER TABLE (continued)

Description	Comment	Byte Address (Hex)	Bits	Data (Binary)	Data (Hex)

Table 15. SFDP PARAMETER TABLE (continued)

Description	Comment	Byte Address (Hex)	Bits	Data (Binary)	Data (Hex)
JDEC BASIC FLASH PARAMETER TABLES (FROM 13th DWORD TO 16th DWORD)					
Program Resume Instruction (Program Operation)	30h (as same as erase resume)	70h	7:0	0011_0000b	30h
Program Suspend Instruction (Program Operation)	B0h (as same as erase suspend)	71h	15:8	1011_0000b	B0h
Resume Instruction (Write or Erase Type Operation)	30h (as same as program resume)	72h	23:16	0011_0000b	30h
Suspend Instruction (Write or Erase Type Operation)	B0h (as same as program suspend)	73h	31:24	1011_0000b	B0h
Reserved		74h	1:0	00b	04h
Status Register Polling Device Busy	Use legacy polling by reading the Status Register with 05h instruction		7:2	0000_01b	
Exit Deep Power Down to Next Operation Delay	40 μs: ((4+1) x 8 μs = 40 μs)	75h	14:8	10_00100b	C4h
Exit Deep Power Down Instruction	ABh		15	1010_1011b	
		76h	22:16		D5h
Enter Deep Power Down Instruction	B9h		23	1011_1001b	
		77h	30:24		5Ch
Deep Power Down Supported	0 = support 1 = not support		31	0b	
(4−4−4) Mode Disable Sequences	−	78h	3:0	0000b	00h
(4−4−4) Mode Enable Sequences	−		7:4	0000b	
		79h	8	0b	00h
(0−4−4) Mode Supported	0 = not support 1 = support		9	0b	
(0−4−4) Mode Exit Method	−		15:10	00_0000b	
(0−4−4) Mode Entry Method	−	7Ah	19:16	0000b	00h
Quad Enable Requirements (QER)	00b: not have a QE bit		22:20	000b	
Hold and WP Disable	0: not supported		23	0b	
Reserved	−	7Bh	31:24		

Table 15. SFDP PARAMETER TABLE (continued)

Description	Comment	Byte Address (Hex)	Bits	Data (Binary)	Data (Hex)
VENDER (ON SEMICONDUCTOR) PARAMETER 1 TABLES (FROM 1th DWORD TO 4th DWORD)					
Supply Maximum Voltage	1900h = 1.900 V 2400h = 2.400 V 1950h = 1.950 V 2700h = 2.700 V 2000h = 2.000 V 3000h = 3.000 V 2200h = 2.200 V 3600h = 3.600 V	C0h C1h	15:0	−	50h 19h
Supply Minimum Voltage	1600h = 1.600 V 20000h = 2.000 V 1650h = 1.650 V 22000h = 2.200 V 1700h = 1.700 V 23000h = 2.300 V 1800h = 1.800 V 27000h = 2.700 V	C2h C3h	31:16	−	50h 16h
RESET Pin	0 = not support 1 = support	C4h	0	0b	14h
RESET Active Logic Level	0 = active logic is 0 1 = active logic is 1		1	0b	
HOLD Pin	0 = not support 1 = support		2	1b	
HOLD Active Logic Level	0 = active logic is 0 1 = active logic is 1		3	0b	
WP Pin	0 = not support 1 = support		4	1b	
WP Active Logic Level	0 = active logic is 0 1 = active logic is 1		5	0b	
Reserved	00b		7:6	00b	
Reserved	All FFh	C5h C6h C7h	31:8	1111_1111b 1111_1111b 1111_1111b	FFh FFh FFh

HOLD FUNCTION

Figure 29.

HOLD Function

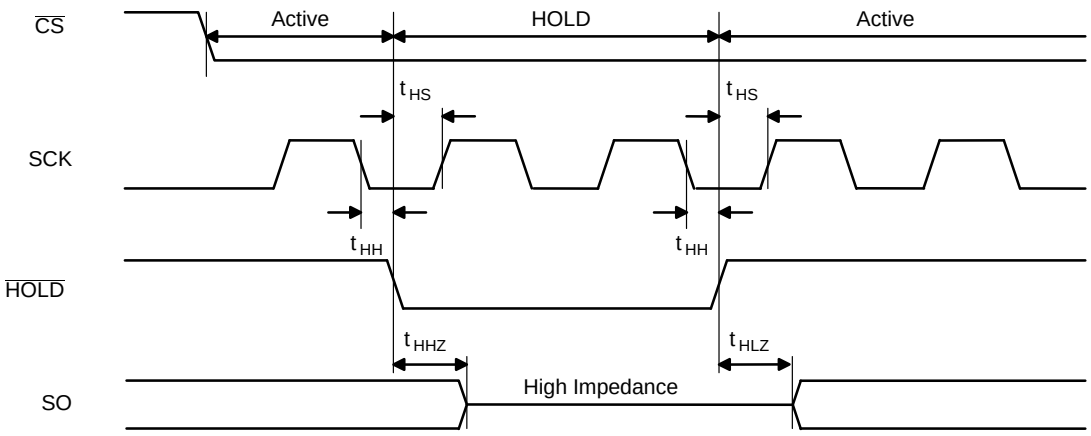


Figure 29. HOLD Function

HARDWARE DATA PROTECTION

–

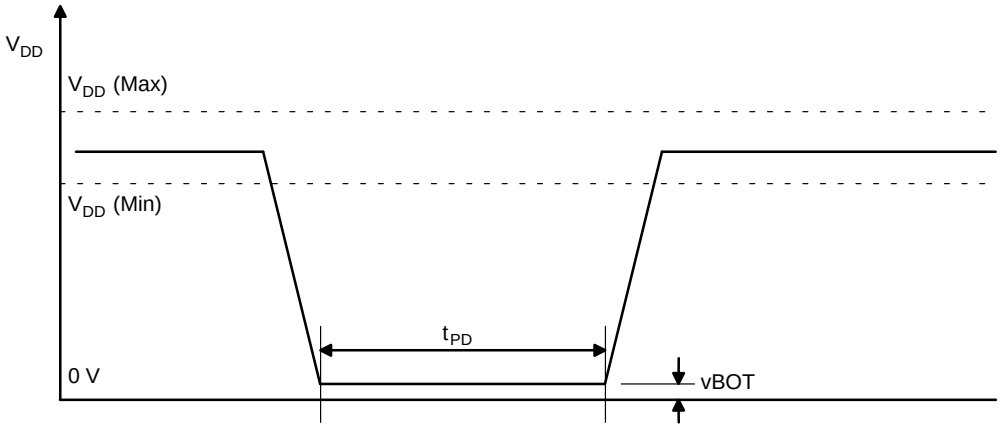


Figure 31. Power−down Timing

Table 17. POWER−DOWN TIMING

Parameter	Symbol	Spec		Unit
		Min	Max	
Power−down Time	t_{PD}	10	−	ms
Power−down Voltage	V_{BOT}	−	0.2	V

SOFTWARE DATA PROTECTION

- —
- –
-

SPECIFICATIONS

Absolute Maximum Ratings

Table 18. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Rating	Unit
Maximum Supply Voltage		With respect to V_{SS}	−0.5 to +2.6	V
DC Voltage (All Pins)		With respect to V_{SS}	−0.5 to V_{DD} + 0.5	V
Storage Temperature	Tstg		−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Operating Conditions

Table 19. OPERATING CONDITIONS

Parameter	Symbol	Conditions	Rating	Unit
Operating Supply Voltage			1.65 to 1.95	V
Operating Ambient Temperature			−40 to +90	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Data Retention, Rewriting Cycles

Table 20. DATA RETENTION, REWRITING CYCLES

Parameter	Symbol	Conditions	Min	Max	Unit
Rewrite Cycles	cycRW	Status resister write	100,000	−	cycles/ Sector
		Program/Erase	100,000	−	
Data Retention	tDRET		20	−	year

Pin Capacitance at Ta = 25°C, f = 1 MHz

Table 21. PIN CAPACITANCE (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Conditions	Rating	Unit
			Max	
Output Pin Capacitance	C_{SO}	V_{SO} = 0 V	12	pF
Input Pin Capacitance	C_{IN}	V_{IN} = 0 V	6	pF

NOTE: These parameter values do not represent the results of measurements undertaken for all devices but rather values for some of the sampled devices.

AC Test Conditions

AC Characteristics

Table 23. AC CHARACTERISTICS

Parameter		Symbol	Rating			Unit
			Min	Typ	Max	
Clock Frequency	Low−Power Read (RDLP: 03h)	f_{CLK}	−	−	33.33	MHz

TIMING WAVEFORMS

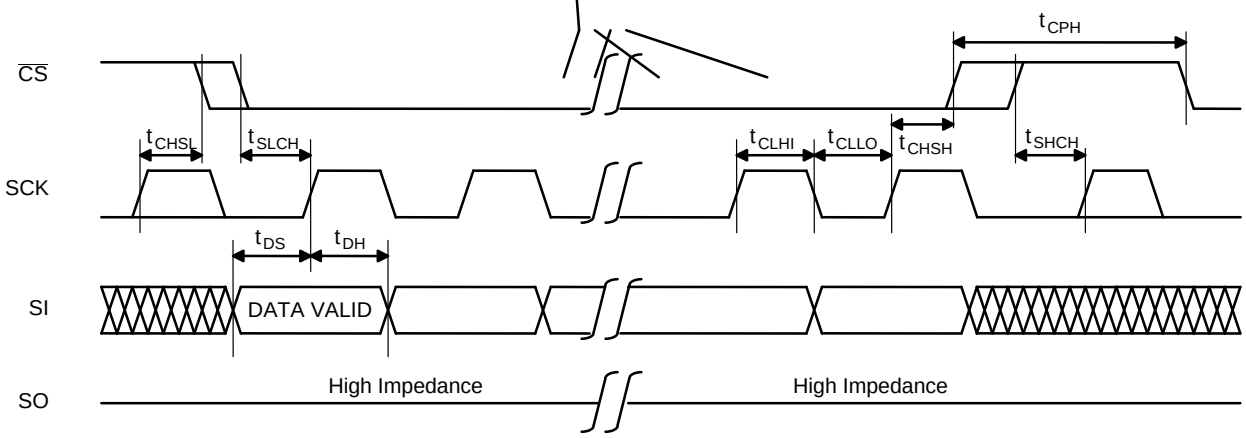


Figure 33. Serial Input Timing

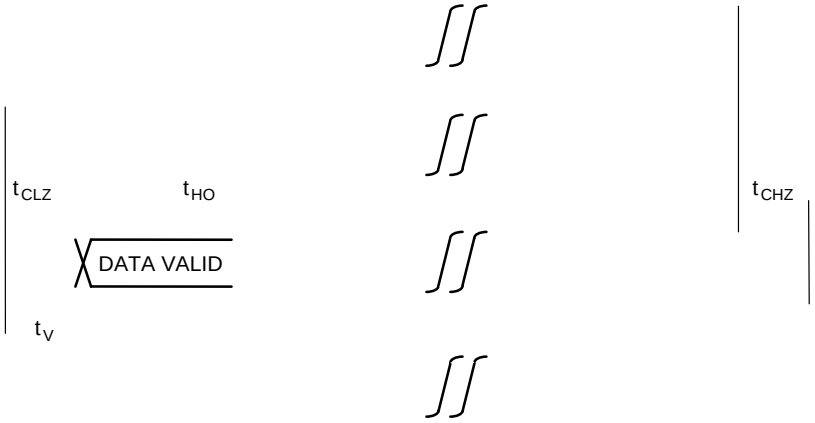


Figure 34. Serial Output Timing

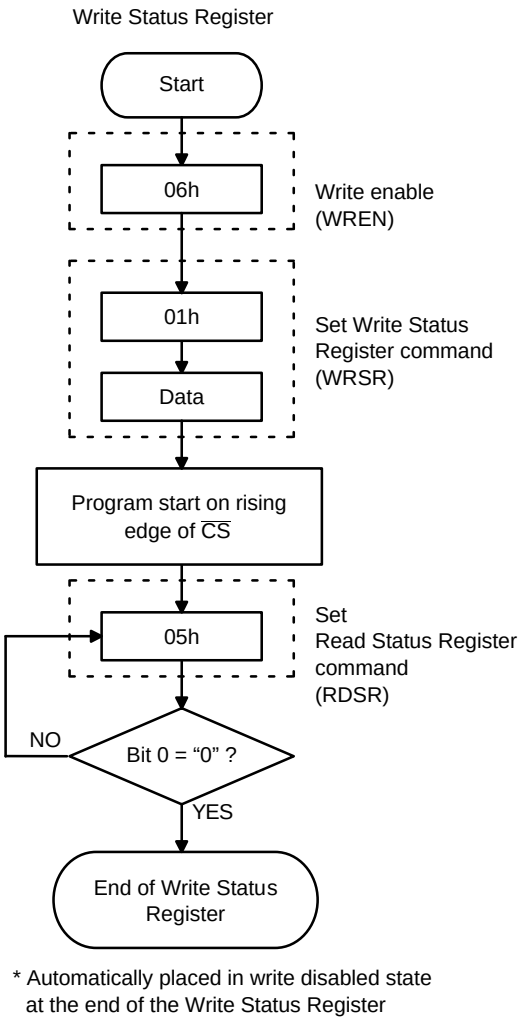


Figure 37. Write Status Register Flowcharts

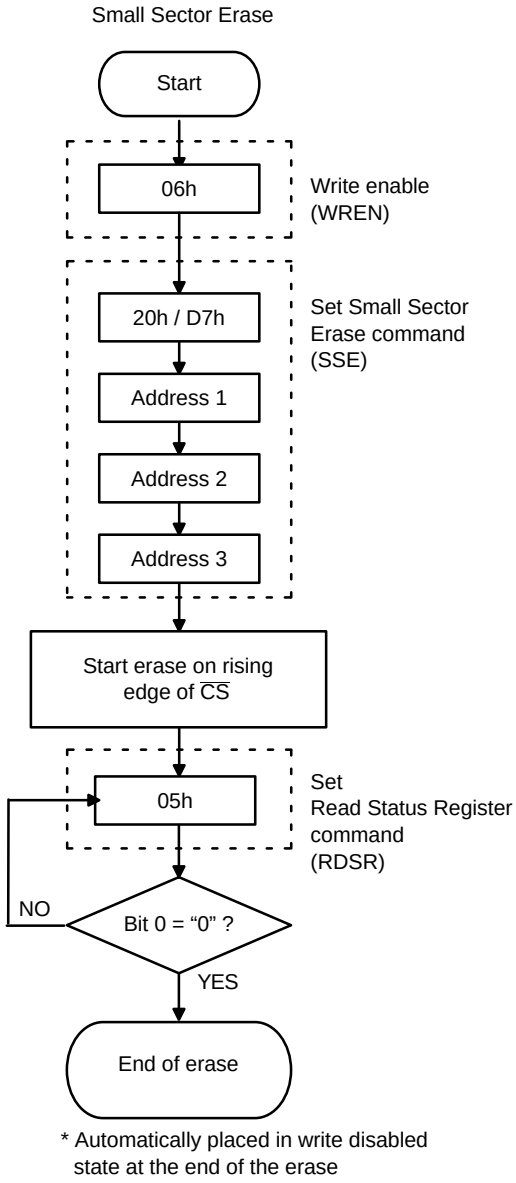


Figure 38. Small Sector Erase Flowcharts

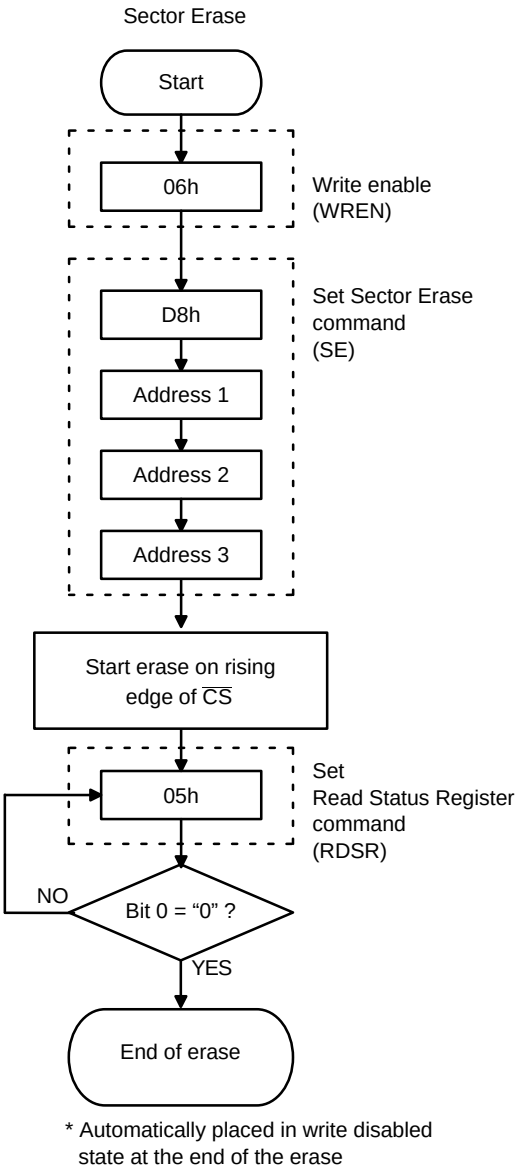


Figure 39. Sector Erase Flowcharts

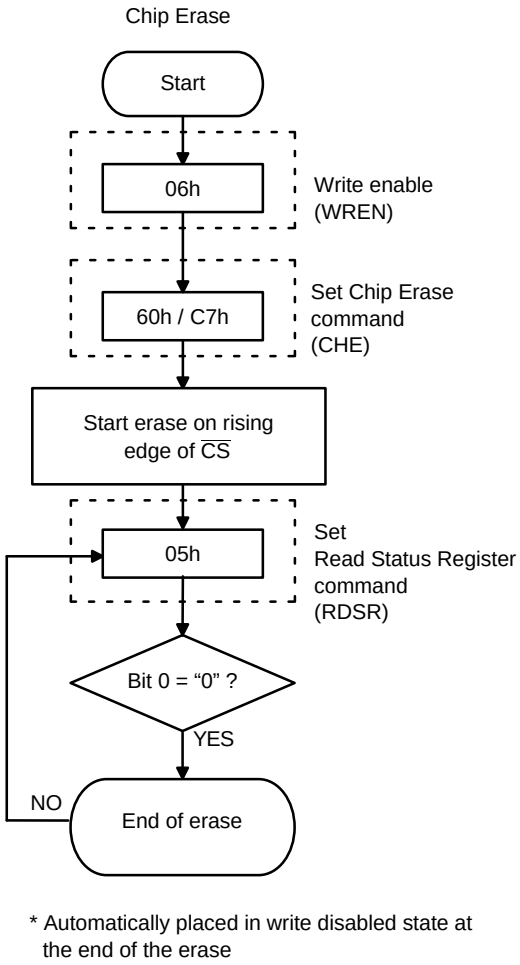


Figure 40. Chip Erase Flowcharts

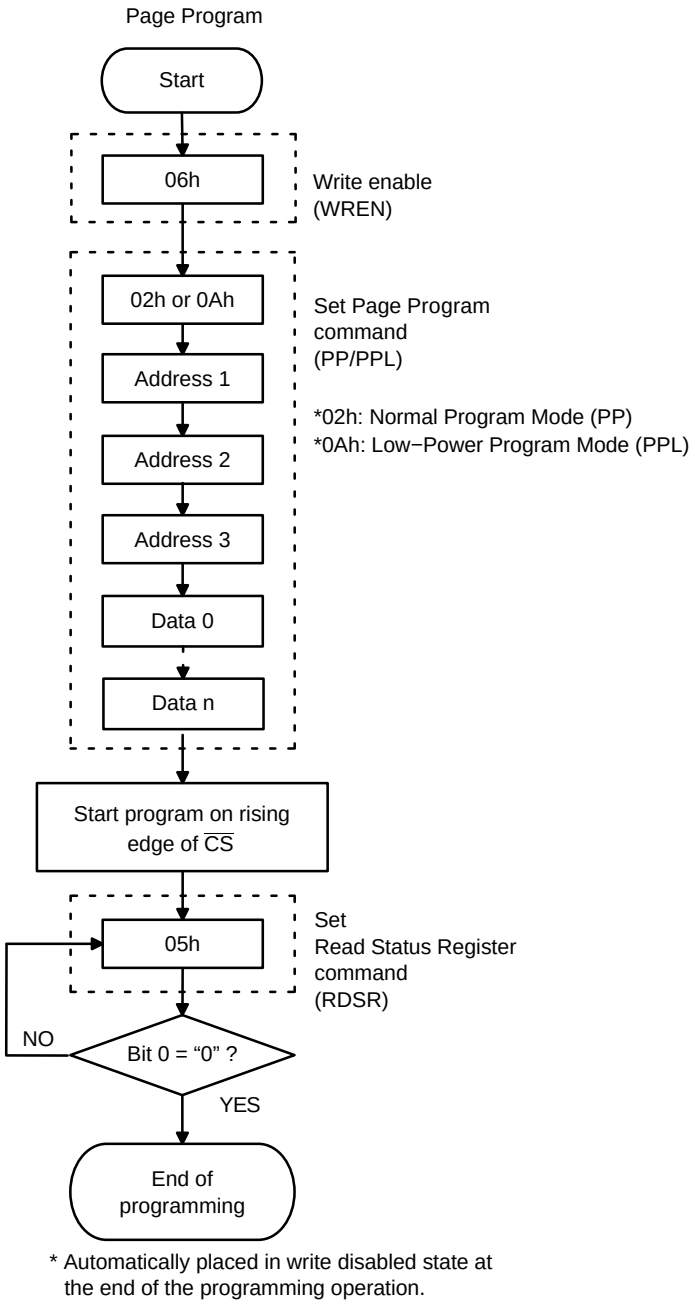


Figure 41. Page Program Flowcharts

CASE 567YR
ISSUE O

DATE 21 NOV 2019

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.