LE25S20XA

Serial Flash Memory
2 Mb (256K x 8)

ON Semiconductor®

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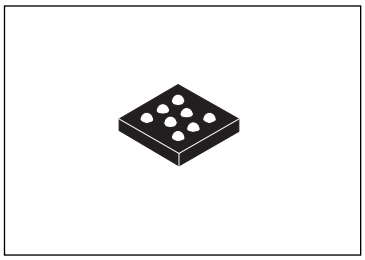
Overview

The LE25S20XA is a SPI bus flash memory device with a 2M bit (256K 8-bit) configuration. It uses a single 1.8V power supply. While making the most of the features inherent to a serial flash memory device, the LE25S20XA is housed in an 8-pin ultra-miniature package. All these features make this device ideally suited to storing program in applications more compact dimensions. The LE25S20XA also has a small sector erase capability which makes the device ideal for storing parameters or data that have fewer rewrite cycles and conventional EEPROMs cannot handle due to insufficient capacity.



WLCSP8, 1.55x1.53

Features

1.

Operations power supply	: 1.65 to 1.95V supply voltage range
Operating frequency	: 40MHz (max)
Temperature range	: –40 to +85 C
Serial interface	: SPI mode 0, mode 3 supported
Electronic Identification	: JDEC ID, Device ID
Sector size	: 4K bytes/small sector, 64K bytes/sector
Erase functions	: Small Sector Erase (SSE), Sector Erase (SE), Chip Erase (CHE)
Page program function	: 256 bytes/page
Status functions	: Ready/Busy information, protect information
Low operation current	: 6.0mA (Read mode operation current ,40MHz)
	:15mA (Erase or Program mode operating current)
	:10uA (CMOS standby current)
Erase time	: 40ms (SSE, typ), 80ms (SE, typ), 300ms (CHE, typ)
Page program time (tPP)	: 3.0ms/256 bytes (typ.), 3.5ms/256 bytes (max.)
High reliability	: 100,000 erase/program cycles
	: 20 years data retention period
Package	: WLCSP8

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ORDERING INFORMATION

See detailed ordering and shipping information on page 24 of this data sheet.

Package Dimensions

unit : mm

Figure 1 Ball Assignments

Ball No.	Symbol	Pin Name
A1	V_{DD}	Power supply
A2	$\overline{HOLD}$	Hold
A3	$\overline{CS}$	Chip select
B1	SCK	Serial clock
B2	SO	Serial data output
C1	SI	Serial data input
C2	$\overline{WP}$	Write protect
C3	V_{SS}	Ground

Figure 2 Block Diagram

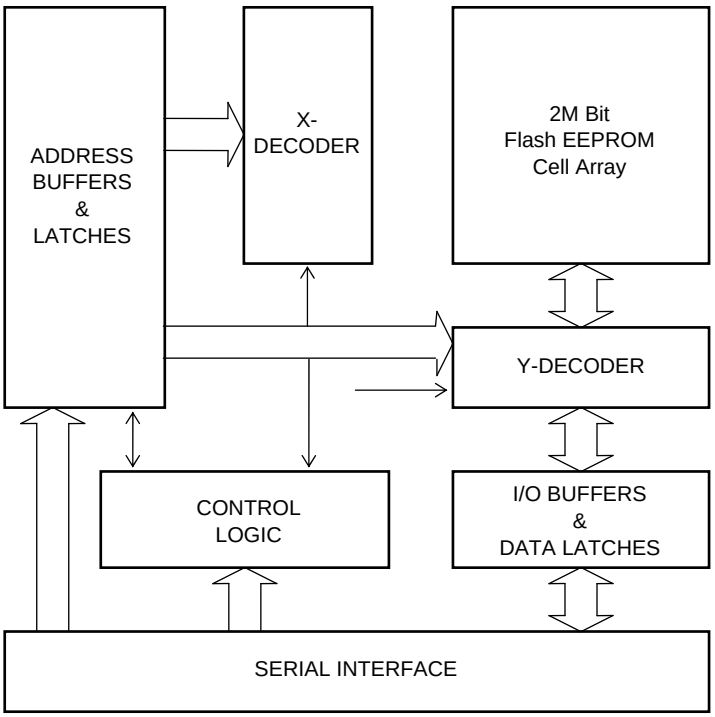


Table 1 Pin Description

Symbol	Pin Name	Description
SCK	Serial clock	This pin controls the data input/output timing. The input data and addresses are latched synchronized to the rising edge of the serial clock, and the data is output synchronized to the falling edge of the serial clock.
SI	Serial data input	The data and addresses are input from this pin, and latched internally synchronized to the rising edge of the serial clock.
SO	Serial data output	The data stored inside the device is output from this pin synchronized to the falling edge of the serial clock.
$\overline{CS}$	Chip select	The device becomes active when the logic level of this pin is low; it is deselected and placed in standby status when the logic level of the pin is high.
$\overline{WP}$	Write protect	The status register write protect (SRWP) takes effect when the logic level of this pin is low.
$\overline{HOLD}$	Hold	Serial communication is suspended when the logic level of this pin is low.
V_{DD}	Power supply	This pin supplies the 1.65 to 1.95V supply voltage.
V_{SS}	Ground	This pin supplies the 0V supply voltage.

Device Operation

The read, erase, program and other required functions of the device are executed through the command registers. The serial I/O corrugate is shown in Figure 3 and the command list is shown in Table 2. At the falling $\overline{CS}$ edge the device is selected, and serial input is enabled for the commands, addresses, etc. These inputs are normalized in 8 bit units and taken into the device interior in synchronization with the rising edge of SCK, which causes the device to execute operation according to the command that is input.

The LE25S20XA supports both serial interface SPI mode 0 and SPI mode 3. At the falling $\overline{CS}$ edge, SPI mode 0 is automatically selected if the logic level of SCK is low, and SPI mode 3 is automatically selected if the logic level of SCK is high.

Figure 3 I/O waveforms

Table 2 Command Settings

Command	1st bus cycle	2nd bus cycle	3rd bus cycle	4th bus cycle	5th bus cycle	6th bus cycle	Nth bus cycle
Read	03h	A23-A16	A15-A8	A7-A0	RD *1	RD *1	RD *1
	0Bh	A23-A16	A15-A8	A7-A0	X	RD *1	RD *1
Small sector erase	20h / D7h	A23-A16	A15-A8	A7-A0			
Sector erase	D8h	A23-A16	A15-A8	A7-A0			
Chip erase	60h / C7h						
Page program	02h	A23-A16	A15-A8	A7-A0	PD *2	PD *2	PD *2

Table 3 Command Settings

2M Bit

sector(64KB)	small sector	address space(A23 to A0)	
3	63	03F000h	03FFFFh
	to		
	48	030000h	030FFFh
2	47	02F000h	02FFFFh
	to		
	32	020000h	020FFFh
1	31	01F000h	01FFFFh
	to		
	16	010000h	010FFFh
0	15	00F000h	00FFFFh
	to		
	2	002000h	002FFFh
	1	001000h	001FFFh
	0	000000h	000FFFh

Description of Commands and Their Operations

A detailed description of the functions and operations corresponding to each command is presented below.

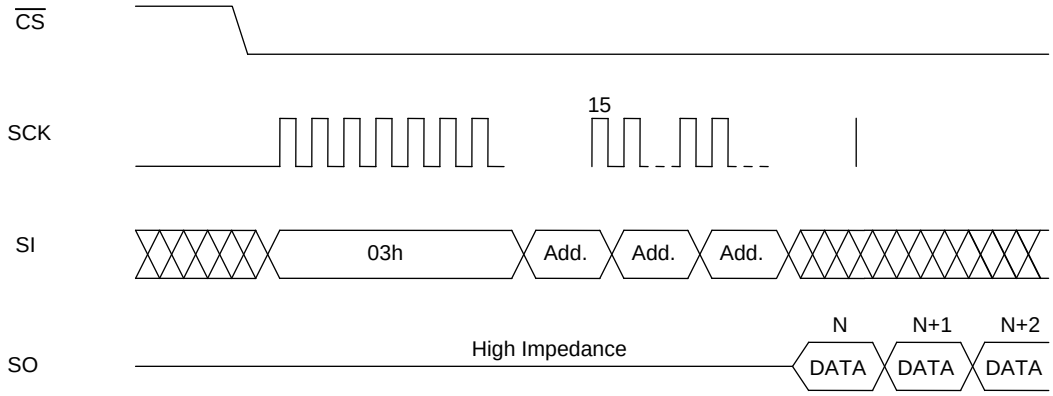
1. Standard SPI read

There are two read commands, the standard SPI read command and High-speed read command.

1-1. Read command

Consisting of the first through fourth bus cycles, the 4 bus cycle read command inputs the 24-bit addresses following (03h). The data is output from SO on the falling clock edge of fourth bus cycle bit 0 as a reference. "Figure 4-a Read" shows the timing waveforms.

Figure 4-a Read



1-2. High-speed Read command

Consisting of the first through fifth bus cycles, the High-speed read command inputs the 24-bit addresses and 8 dummy bits following (0Bh). The data is output from SO using the falling clock edge of fifth bus cycle bit 0 as a reference. "Figure 4-b High-speed Read" shows the timing waveforms.

Figure 4-b High-speed Read

When SCK is input continuously after the read command has been input and the data in the designated addresses has been output, the address is automatically incremented inside the device while SCK is being input, and the corresponding data is output in sequence. If the SCK input is continued after the internal address arrives at the highest address (3FFFFh), the internal address returns to the lowest address (00000h), and data output is continued. By setting the logic level of $\overline{CS}$ to high, the device is deselected, and the read cycle ends. While the device is deselected, the output pin SO is in a high-impedance state.

2. Status Registers

The status registers hold the operating and setting statuses inside the device, and this information can be read (status register read) and the protect information can be rewritten (status register write). There are 8 bits in total, and "Table 4 Status registers" gives the significance of each bit.

Table 4 Status Registers

Bit	Name	Logic	Function	Power-on Time Information
Bit0	$\overline{\text{RDY}}$	0	Ready	0
		1	Erase/Program	
Bit1	WEN	0	Write disabled	0
		1	Write enabled	
Bit2	BP0	0	Block protect information	

2-2. Status register write

The information in status registers BP0, BP1, BP2, TB and SRWP can be rewritten using the status register write command. RDY, WEN and bit 6 are read-only bits and cannot be rewritten. The information in bits BP0, BP1, BP2, TB and SRWP is stored in the non-volatile memory, and when it is written in these bits, the contents are retained even at power-down. "Figure 6 Status Register Write" shows the timing waveforms of status register write, and Figure 19 shows a status register write flowchart. Consisting of the first and second bus cycles, the status register write command initiates the internal write operation at the rising CS edge after the data has been input

BP0, BP1, BP2, TB (Bits 2, 3, 4, 5)

Block protect BP0, BP1, BP2 and TB are status register bits that can be rewritten, and the memory space to be protected can be set depending on these bits. For the setting conditions, refer to "Table 5 Protect level setting conditions".

BP0, BP1, and BP2 are used to select the protected area and TB to allocate the protected area to the higher-order address area or lower-order address area.

Table 5 Protect Level Setting Conditions

Protect Level	Status Register Bits			Protected Area
	TB	BP1	BP0	

4. Write Disable

The write disable command sets status register WEN to "0" to prohibit unintentional writing. "Figure 8 Write Disable" shows the timing waveforms. The write disable co

6. Small Sector Erase

Small sector erase is an operation that sets the memory cell data in any small sector to "1". A small sector consists of
4Kbytes. "Figure 11 Small Sector Erase" shows the timi

8. Chip Erase

Chip erase is an operation that sets the memory cell data in all the sectors to "1". "Figure 13 Chip Erase" shows the timing waveforms, and Figure 20 shows a chip erase flowchart. The chip erase command consists only of the first bus cycle, and it is initiated by inputting (60h) or (C7h). After the command has been input, the internal erase operation starts from the rising $\overline{CS}$ edge, and it ends automatically by the control exercised by the internal timer. Erase end can also be detected using status register $\overline{RDY}$.

Figure 13 Chip Erase

9. Page Program

Page program is an operation that programs any number of bytes from 1 to 256 bytes within the same sector page (page addresses: A17 to A8). Before initiating page program, the data on the page concerned must be erased using small sector erase, sector erase, or chip erase. "Figure 14 Page Program" shows the page program timing waveforms, and Figure 21 shows a page program flowchart. After the falling $\overline{CS}$, edge, the command (02H) is input followed by the 24-bit addresses. Addresses A17 to A0 are valid. The program data is then loaded at each

10. Silicon ID Read

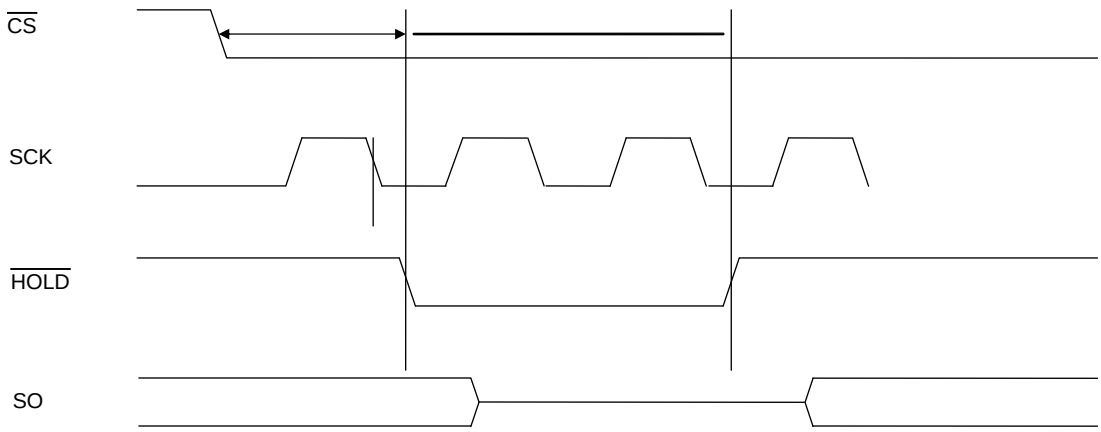
ID read is an operation that reads the manufacturer code and device ID information. The silicon ID read command is not accepted during writing. There are two methods of reading the silicon ID, each of which is assigned a device ID. In the first method, the read command sequence consists only of the first bus cycle in which (9Fh) is input. In the subsequent bus cycles, the manufacturer code 62h which is assigned by JEDEC, 2-byte device ID code (memory type, memory capacity), and reserved code are output sequentially. The 4-byte code is output repeatedly as long as clock inputs are present, "Table 7-1 JEDEC ID code " lists the silicon ID codes and "Figure 15-a JEDEC ID read" shows the JEDEC ID read timing waveforms.

The second method involves inputting the ID read commanru25.3()-2(e m)1ID .3((ru25.3()-read)-5.3(co)-5.3(mman)]TJ24.4551 0

11. Hold Function

Using the $\overline{\text{HOLD}}$ pin, the hold function suspends serial communication (it places it in the hold status). "Figure16 $\overline{\text{HOLD}}$" shows the timing waveforms. The device is placed in the hold status at the falling $\overline{\text{HOLD}}$ edge while the logic level of SCK is low, and it exits from the hold status at the rising $\overline{\text{HOLD}}$ edge. When the logic level of SCK is high, $\overline{\text{HOLD}}$ must not rise or fall. The hold function takes effect when the logic level of $\overline{\text{CS}}$ is low, the hold status is exited and serial communication is reset at the rising $\overline{\text{CS}}$ edge. In the hold status, the SO output is in the high-impedance state, and SI and SCK are "don't care".

Figure 16 $\overline{\text{HOLD}}$



12. Power-on

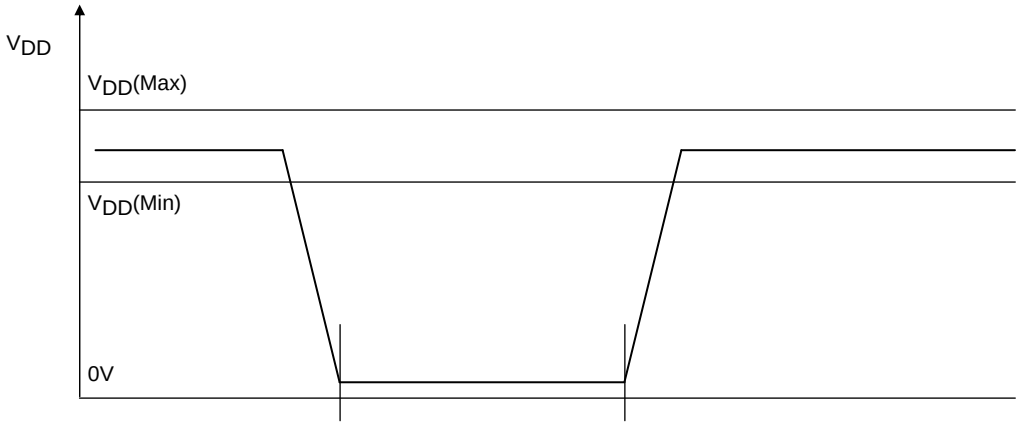
In order to protect against unintentional writing, $\overline{\text{CS}}$ must be within at V_{DD} 0.3 to V_{DD}+0.3 on power-on. After power-on, the supply voltage has stabilized at VDD min. or higher, waits for t_{PU} before inputting the command to start a device operation. The device is in the standby state and not in the power-down state after power is turned on. To put the device into the power-down state, it is necessary to enter a power-down command.

Figure 17 Power-on Timing

13. Hardware Data Protection

LE25S20XA incorporates a power-on reset function. The following conditions must be met in order to ensure that the power reset circuit will operate stably.
No guarantees are given for data in the event of an instantaneous power failure occurring during the writing period.

Figure 18 Power-down Timing



Power-on timing

Parameter	Symbol	spec		unit
		min	max	
power-on to operation time	t_{PU}	100		μs
power-down time	t_{PD}	10		ms
power-down voltage	t_{BOT}		0.2	V

14. Software Data Protection

The LE25S20XA eliminates the possibility of unintentional operations by not recognizing commands under the following conditions.

When a write command is input and the rising $\overline{CS}$ edge timing is not in a bus cycle (8 CLK units of SCK)
When the page program data is not in 1-byte increments
When the status register write command is input for 2 bus cycles or more

15. Decoupling Capacitor

A 0.1 F ceramic capacitor must be provided to each device and connected between V_{DD} and V_{SS} in order to ensure that the device will operate stably.

Specifications

Absolute Maximum Ratings

AC Characteristics

Parameter			Symbol	Ratings			unit
				min	typ	max	
Clock frequency	Read instruction(03h)		f_{CLK}			25	MHz
	All instructions except for read(03h)					40	MHz
Input signal rising/falling time			t_{RF}	0.1			V/ns
SCK logic high level pulse width		25MHz	t_{CLHI}	14			ns
		40MHz		11.5			
SCK logic low level pulse width		25MHz	t_{CLLO}	14			ns
		40MHz		11.5			
$\overline{CS}$ setup time			t_{CSS}	10			ns
$\overline{CS}$ hold time			t_{CSH}	10			ns
Data setup time			t_{DS}	5			ns
Data hold time			t_{DH}	5			ns
$\overline{CS}$ wait pulse width			t_{CPH}	25			ns
Output high impedance time from $\overline{CS}$			t_{CHZ}			15	ns
Output data time from SCK			t_V		8	11	ns
Output data hold time			t_{HO}	1			ns
Output low impedance time from SCK			t_{CLZ}	0			ns
$\overline{WP}$ setup time			t_{WPS}	20			ns
$\overline{WP}$ hold time			t_{WPH}	20			ns
$\overline{HOLD}$ setup time			t_{HS}	5			ns
$\overline{HOLD}$ hold time			t_{HH}	5			ns
Output low impedance time from $\overline{HOLD}$			t_{HLZ}			12	ns
Output high impedance time from $\overline{HOLD}$			t_{HHZ}			9	ns
Power-down time			t_{DP}			5	s
Power-down recovery time			t_{PRB}			5	s
Write status register time			t_{SRW}		8	10	ms
Page programming cycle time		256Byte	t_{PP}		3	3.5	ms
		nByte			0.15+ n*2.85/256	0.20+ n*3.30/256	ms
Small sector erase cycle time			t_{SSE}		0.04	0.15	s
Sector erase cycle time			t_{SE}		0.08	0.25	s
Chip erase cycle time			t_{CHE}		0.3	3.0	s

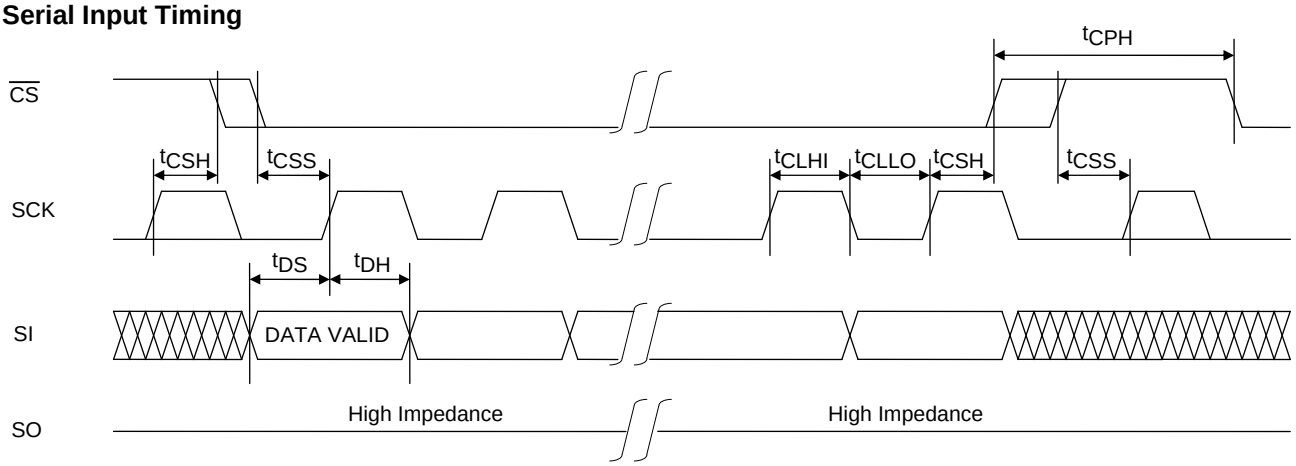
AC Test Conditions

Input pulse level····· $0.2V_{DD}$ to $0.8V_{DD}$
Input rising/falling time ···· 5ns
Input timing level ····· $0.3V_{DD}$, $0.7V_{DD}$
Output timing level ····· 1/2 V_{DD}
Output load ····· 15pF

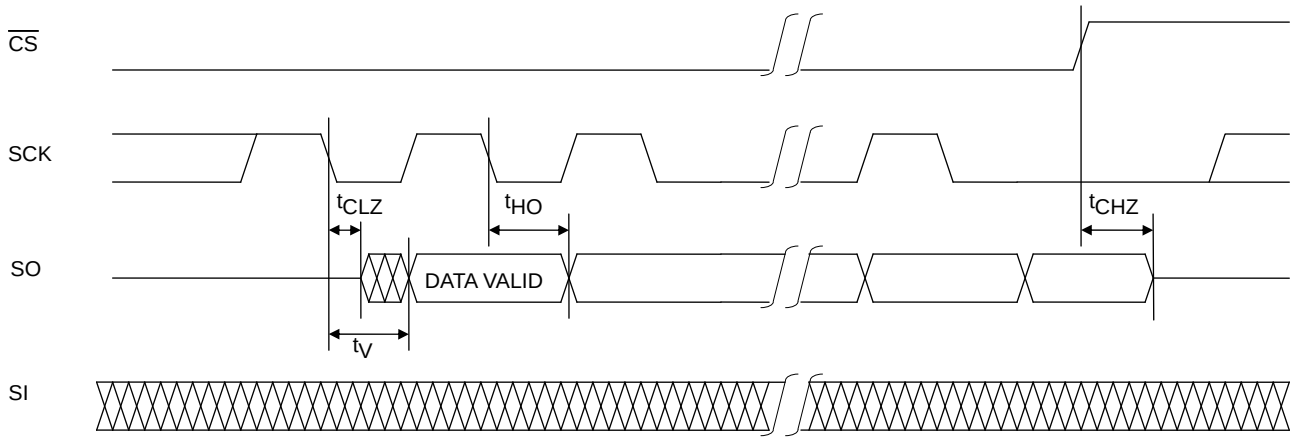
Note: As the test conditions for "typ"-4.5(te: 976 TD tes2137 11e4Tw(976 TD0 Tc( )Tj15.3054 -1.2455 TD.002lf("-4.5(te: 976 3(/fa

Timing waveforms

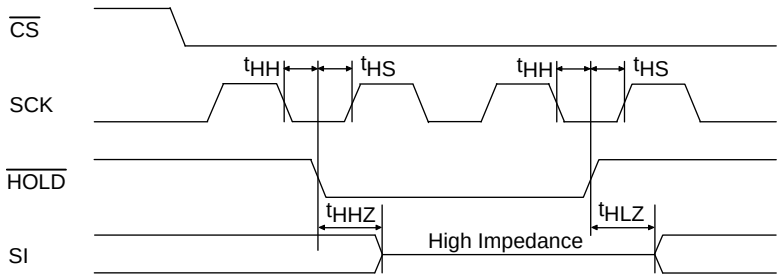
Serial Input Timing



Serial Output Timing



Hold Timing



Status register write Timing

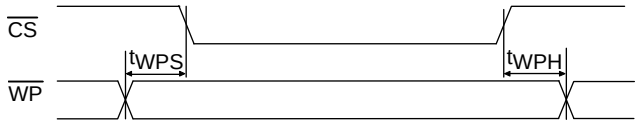
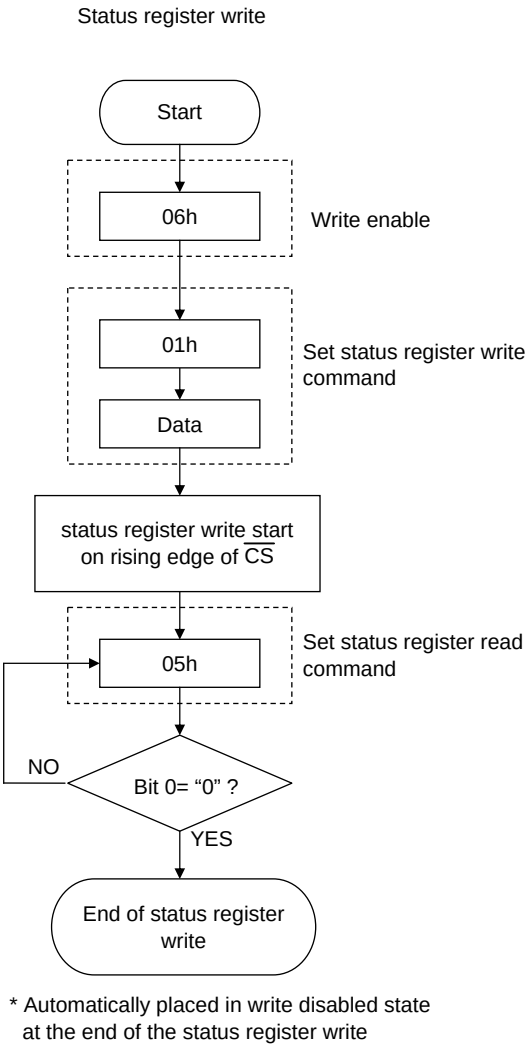
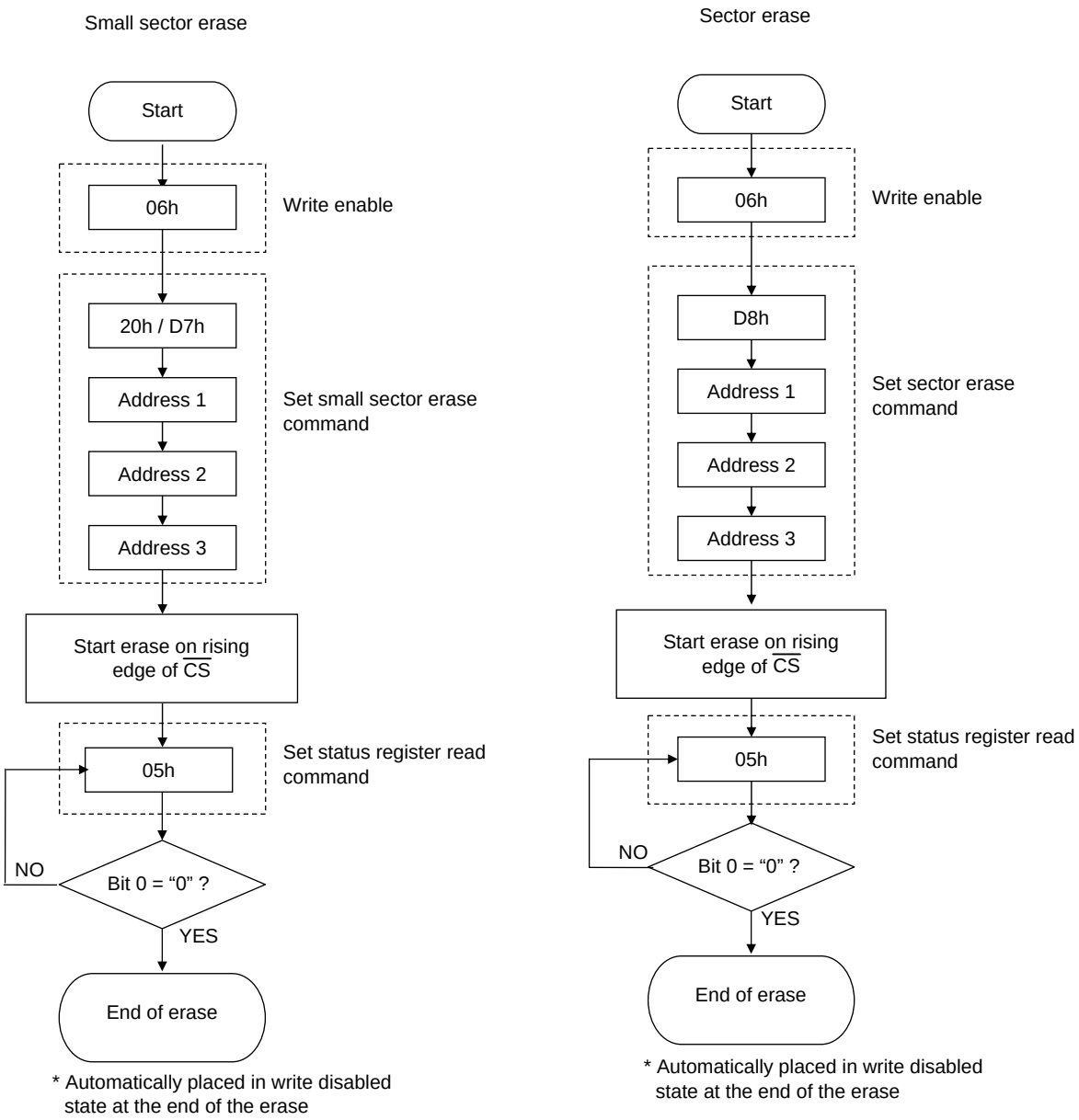


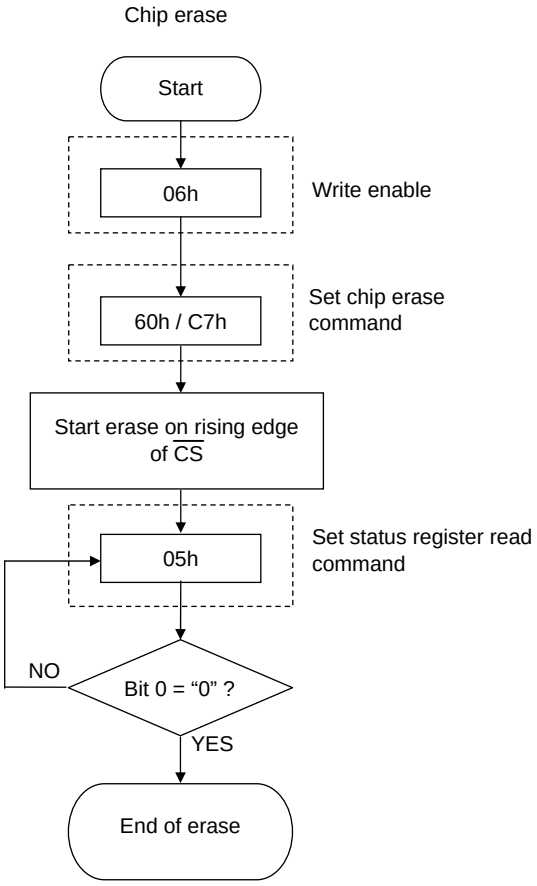
Figure 19 Status Register Write Flowchart



* Automatically placed in write disabled state at the end of the status register write

Figure 20 Erase Flowcharts





* Automatically placed in write disabled state at the end of the erase