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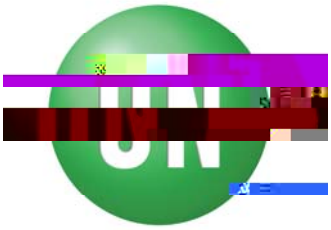
LE25U20AFD

Serial Flash Memory
2 Mb (256K x 8)



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Overview

The LE25U20AFD is a serial interface-compatible flash memory device with a 256K 8-bit configuration. It uses a single 2.5 V power supply. While making the most of the features inherent to a serial flash memory device, the LE25U20AFD is housed in an 8-pin ultra-miniature package. These features make this device ideally suited to storing program codes in applications such as portable information devices, which are required to have increasingly more compact dimensions. Moreover, by using the small sector erase function this product is also suitable for the parameter or the date storage usage with comparatively little rewriting times that becomes a capacity shortage in EEPROM.

Features

Read / write operations enabled by single 2.5 V power supply :
2.30 to 3.60 V supply voltage range
Operating frequency : 30 MHz
Temperature range :

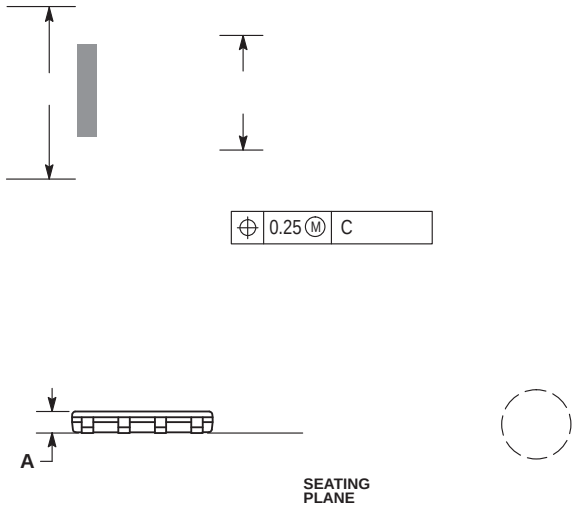
* This product is licensed from Silicon Storage Technology, Inc. (USA).

ORDERING INFORMATION
See detailed ordering and shipping information on page 21 of this data sheet.

Package Dimensions

unit : mm

VSOIC8 NB
CASE 753AA
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE. DIMENSION E DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
5. DATUMS A AND B ARE TO BE DETERMINED AT DATUM F.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

	MILLIMETERS	
DIM	MIN	MAX
A	0.65	0.85
A1	–––	0.05
b	0.31	0.51

e	1.27 BSC

GENERIC
MARKING DIAGRAM*

*This inff3ener9 0 er.59]1c973 41749]AAA

Figure 1 Pin Assignments

Figure 2 Block Diagram

Table 1 Pin Description

Device Operation

The LE25U20AFD features electrical on-chip erase functions using a single 2.5 V power supply, that have been added to the EPROM functions of the industry standard that support serial interfaces. Interfacing and control are facilitated by incorporating the command registers inside the chip. The read, erase, program and other required functions of the device are executed through the command registers. The command addresses and data input in accordance with "Table 2 Command Settings" are latched inside the device in order to execute the required operations. "Figure 3 Serial Input Timing" shows the timing waveforms of the serial data input. First, at the falling $\overline{CS}$ edge the device is selected, and serial input is enabled for the commands, addresses, etc. These inputs are introduced internally in sequence starting with bit 7 in synchronization with the rising SCK edge. At this time, output pin SO is in the high-impedance state. The output pin is placed in the low-impedance state when the data is output in sequence starting with bit 7 synchronized to the falling clock edge during read, status register read and silicon ID. Refer to "Figure 4 Serial Output Timing" for the serial output timing.

The LE25U20AFD supports both serial interface SPI mode 0 and SPI mode 3. At the falling $\overline{CS}$ edge, SPI mode 0 is automatically selected if the logic level of SCK is low, and SPI mode 3 is automatically selected if the logic level of SCK is high.

Table 2 Command Settings

Command	1st bus cycle	2nd bus cycle	3rd bus cycle	4th bus cycle	5th bus cycle	6th bus cycle	Nth bus cycle
Read	03h	A23-A16	A15-A8	A7-A0			
	0Bh	A23-A16	A15-A8	A7-A0	X		

Figure 3 Serial Input Timing

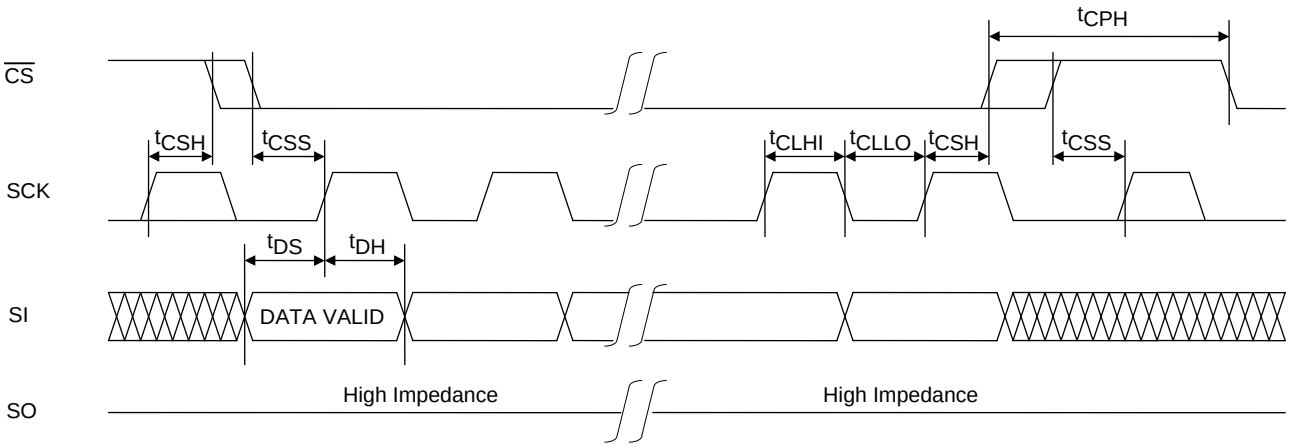
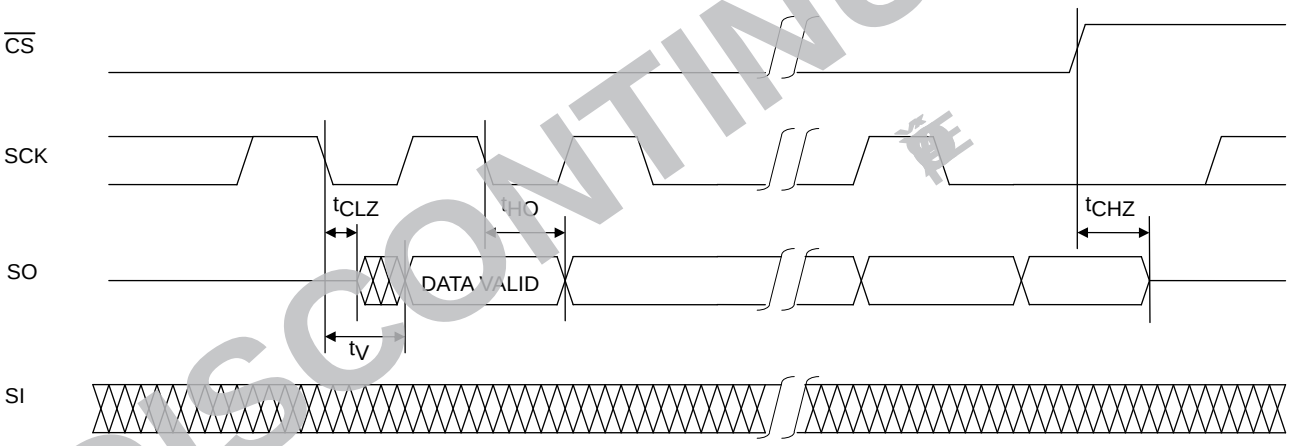


Figure 4 Serial Output Timing



Description of Commands and Their Operations

"Table 2 Command Settings" provides a list and overview of the commands. A detailed description of the functions and operations corresponding to each command is presented below.

1. Read

There are two read commands, the 4 bus cycle read command and 5 bus cycle read command. Consisting of the first through fourth bus cycles, the 4 bus cycle read command inputs the 24-bit addresses following (03h), and the data in the designated addresses is output synchronized to SCK. The data is output from SO on the falling clock edge of fourth bus cycle bit 0 as a reference. "Figure 5-a 4 Bus Read" shows the timing waveforms.

Consisting of the first through fifth bus cycles, the 5 bus cycle read command inputs the 24-bit addresses and 8 dummy bits following (0Bh). The data is output from SO using the falling clock edge of fifth bus cycle bit 0 as a reference. "Figure 5-b 5 Bus Read" shows the timing waveforms. The only difference between these two commands is whether the dummy bits in the fifth bus cycle are input.

When SCK is input continuously after the read command has been input and the data in the designated addresses has been output, the address is automatically incremented inside the device while SCK is being input, and the corresponding data is output in sequence. If the SCK input is continued after the internal address arrives at the highest address (3FFFFh), the internal address returns to the lowest address (00000h), and data output is continued. By setting the logic level of $\overline{CS}$ to high, the device is deselected, and the read cycle ends. While the device is deselected, the output pin SO is in a high-impedance state.

Figure 5-a 4 Bus Read

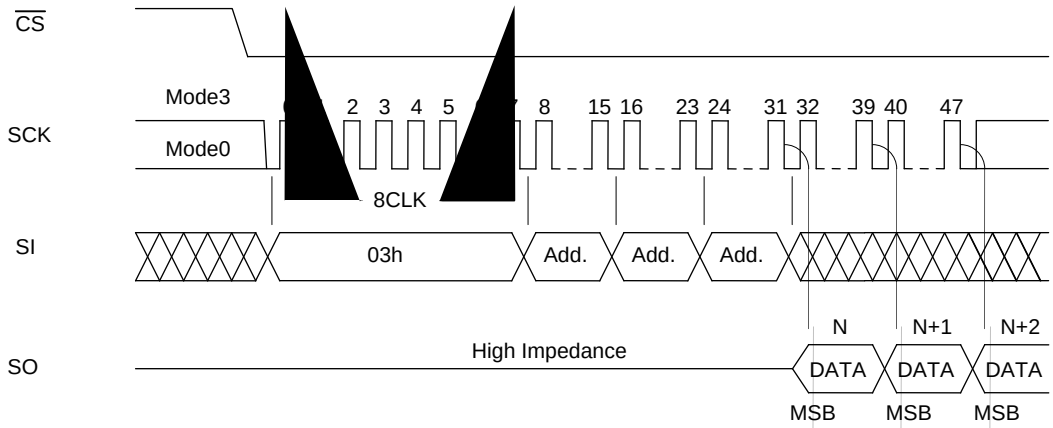
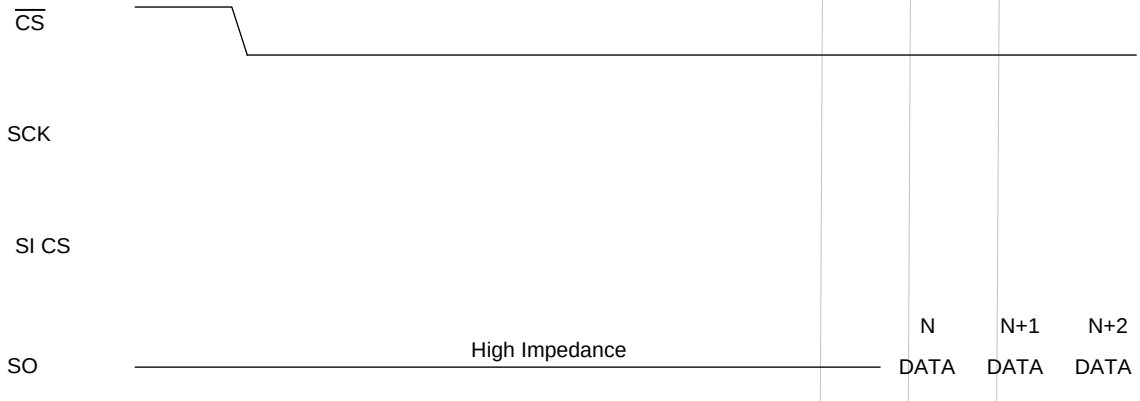


Figure 5-b 5 Bus Read



2. Status Registers

The status registers hold the operating and setting statuses inside the device, and this information can be read (status register read) and the protect information can be rewritten (status register write). There are 8 bits in total, and "Table 3 Status registers" gives the significance of each bit.

Table 3 Status Registers

Bit	Name	Logic	Function	Power-on Time Information
Bit0	$\overline{\text{RDY}}$	0	Ready	0
		1	Erase/Program	
Bit1	WEN	0	Write disabled	

2-2. Status Register Write

The information in status registers BP0, BP1, and SRWP can be rewritten using the status register write command. RDY, WEN, bit 4, bit 5, and bit 6 are read-only bits and cannot be rewritten. The information in bits BP0, BP1, and SRWP is stored in the non-volatile memory, and when it is written in these bits, the contents are retained even at power-down. "Figure 7 Status Register Write" shows the timing waveforms of status register write, and Figure 20 shows a status register write flowchart. Consisting of the first and second bus cycles, the status register write command initiates the internal write operation at the rising CS edge after the data has been input following (01h). Erase and program are performed automatically inside the device by status register write so that erasing or other processing is unnecessary before executing the command. By the operation of this command, the information in bits BP0, BP1, and SRWP can be rewritten. Since bits RDY (bit 0), WEN (bit 1), bit 4, bit 5, and bit 6 of the status register cannot berei bS7 (Si)7.2w1ne 7.2gu willre i an ca6.9m.9 3pnmdedeedewhe teBP. C.2 (d) S3.4 3ath. . ehbe re (d)-e3.4 3ee

WEN (bit 1)

Th6t.7 4stwng 6 (w)pe5 4 (ngf3 d6 r)-13rr81c.64245 T[Thopt)3 5 rw w

3. Write Enable

Before performing any of the operations listed below, the device must be placed in the write enable state. Operation is the same as for setting status register WEN to "1", and the state is enabled by inputting the write enable command. "Figure 8 Write Enable" shows the timing waveforms when the write enable operation is performed. The write enable command consists only of the first bus cycle, and it is initiated by inputting (06h).

Small sector erase, sector erase, chip erase
Page program
Status register write

4. Write Disable

The write disable command sets status register WEN to "0" to prohibit unintentional writing. "Figure 9 Write Disable" shows the timing waveforms. The write disable command consists only of the first bus cycle, and it is initiated by inputting (04h). The write disable state (WEN "0") is exited by setting WEN to "1" using the write enable command (06h).

Figure 8 Write Enable

Figure 9 Write Disable

5. Power-down

The power-down command sets all the commands, with the

6. Small Sector Erase

Small sector erase is an operation that sets the memory cell data in any small sector to "1". A small sector consists of 4K bytes. "Figure 12 Small Sector Erase" shows the timing waveforms, and Figure 21 shows a small sector erase flowchart. The small sector erase command consists of the first through fourth bus cycles, and it is initiated by inputting the 24-bit addresses following (D7h/20h). Addresses A17 to A12 are valid, and Addresses A23 to A18 are "don't care". After the command has been input, the internal erase operation starts from the rising $\overline{CS}$ edge, and it ends automatically by the control exercised by the internal timer. Erase end can also be detected using status register $\overline{RDY}$.

Figure 12 Small Sector Erase

7. Sector Erase

Sector erase is an operation that sets the memory cell data in any sector to "1". A sector consists of 64K bytes. "Figure 13 Sector Erase" shows the timing waveforms, and Figure 21 shows a sector erase flowchart. The sector erase command consists of the first through fourth bus

8. Chip Erase

Chip erase is an operation that sets the memory cell data in all the sectors to "1". "Figure 14 Chip Erase" shows the timing waveforms, and Figure 21 shows a chip erase flowchart. The chip erase command consists only of the first bus cycle, and it is initiated by inputting (C7h). After the command has been input, the internal erase operation starts from the rising $\overline{CS}$ edge, and it ends automatically by the control exercised by the internal timer. Erase end can also be detected using status register $\overline{RDY}$.

Figure 14 Chip Erase

9. Page Program

Page program is an operation that programs any number of bytes from 1 to 256 bytes within the same sector page (page addresses: A17 to A8). Before initiating page program, the data on the page concerned must be erased using small sector erase, sector erase, or chip erase. "Figure 15 Page Program" shows the page program timing waveforms, and Figure 22 shows a page program flowchart. After the falling $\overline{CS}$, edge, the command (02H) is input followed by the 24-bit addresses. Addresses A17 to A0 are valid. The program data is then loaded at each rising clock edge until the rising $\overline{CS}$ edge, and data loading is continued until the rising $\overline{CS}$ edge. If the data loaded has exceeded 256 bytes, the 256 bytes loaded last are programmed. The program data must be loaded in 1-byte increments, and the program operation is not performed at the rising $\overline{CS}$ edge occurring at any other timing. The page program time is 2.0 ms (typ.) when 256 bytes (1 page) are programmed at one time.

10. Silicon ID Read

Silicon ID read is an operation that reads the manufacturer code and device code information. The silicon ID read command is not accepted during writing.

Two methods are used for silicon ID reading. The first method involves inputting the 9Fh command: the setting is completed with only the first bus cycle input, and in subsequent bus cycles the manufacturer code 62h, 2 bytes of device ID code (Memory type, Memory capacity) and reserved code are repeatedly output in succession so long as the clock input is continued. Refer to "Figure 16-a Silicon ID Read 1" for the waveforms. "Table 6_1 Silicon ID Read 1" lists the silicon ID read1 codes.

The second method involves inputting the ABh command. This command consists of the first through fourth bus cycles, and the 1 byte silicon ID can be read when 24 dummy bits are input after (ABh). Refer to "Figure 16-b Silicon ID Read 2" for the waveforms. "Table 6_2 Silicon ID Read 2" lists the silicon ID read2 code. If, after the

13. Hardware Data Protection

In order to protect against unintentional writing at power-on, the LE25U20AFD incorporates a power-on reset function. The following conditions must be met in order to ensure that the power reset circuit will operate stably.
No guarantees are given for data in the event of an instantaneous power failure occurring during the writing period.

Figure 19 Power-down Timing

14. Software Data Protection

The LE25U20AFD eliminates the possibility of unintentional operations by not recognizing commands under the following conditions.

When a write command is input and the rising $\overline{CS}$ edge timing is not in a bus cycle (8 CLK units of SCK)

Specifications

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Ratings	unit
Maximum supply voltage	V_{DD} max	With respect to V_{SS}	0.5 to +4.6	V
DC voltage (all pins)	VIN/VOUT	With respect to V_{SS}	0.5 to V_{DD}+0.5	V
Storage temperature	Tstg		55 to +150	C

AC Characteristics

Parameter	Symbol	Ratings			unit
		min	typ	max	
Clock frequency	f_{CLK}			30	MHz
SCK logic high level pulse width	t_{CLHI}	16			ns
SCK logic low level pulse width	t_{CLLO}	16			ns
Input signal rising/falling time	t_{RF}			20	ns
$\overline{CS}$ setup time	t_{CSS}	10			ns

CS

Figure 20 Status Register Write Flowchart

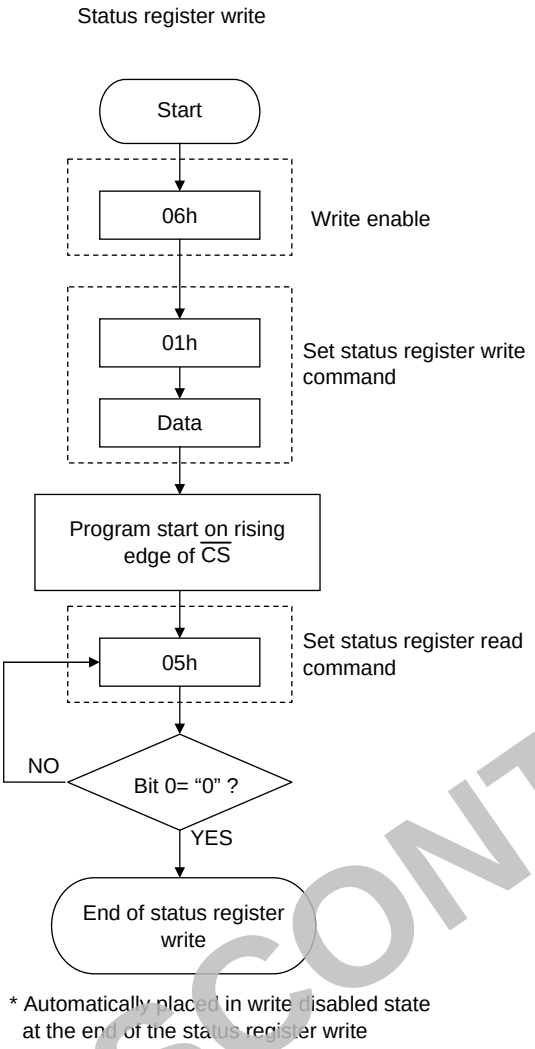


Figure 21 Erase Flowcharts

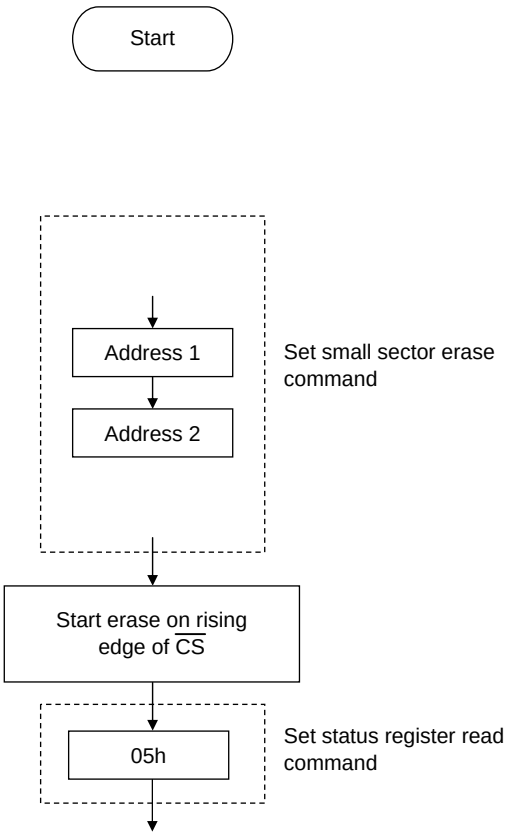


Figure 22 Page Program Flowchart