LE25U20AMB

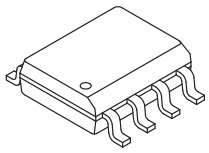
Serial Flash Memory
2 Mb (256K x 8)

ON Semiconductor®

www.onsemi.com

Overview

The LE25U20AMB is a serial interface-compatible flash memory device with a 256K 8-bit configuration. It uses a single 2.5 V power supply. While making the most of the features inherent to a serial flash memory device, the LE25U20AMB is housed in an 8-pin ultra-miniature package. These features make this device ideally suited to storing program codes in applications such as portable information devices, which are required to have increasingly more compact dimensions. Moreover, by using the small sector erase function this product is also suitable for the parameter or the date storage usage with comparatively little rewriting times that becomes a capacity shortage in EEPROM.



SOIC-8 / SOP8K (200 mil)

Features

Read / write operations enabled by single 2.5 V power supply :
2.30 to 3.60 V supply voltage range
Operating frequency : 30 MHz
Temperature range : 40 to +85 C
Serial interface : SPI mode 0, mode 3 supported
Sector size : 4K bytes/small sector, 64K bytes/sector
Small sector erase, sector erase, chip erase functions
Page program function (256 bytes / page)
Block protect function
Status functions : Ready/busy information, protect information
Highly reliable read/write
- Number of rewrite times : 100,000 times
- Small sector erase time : 40 ms (typ), 150 ms (max)
- Sector erase time : 80 ms (typ), 250 ms (max)
- Chip erase time : 250 ms (typ), 1.6 s (max)
- Page program time : 4.0 ms / 256 bytes (typ), 5.0 ms / 256 bytes (max)

Data retention period : 20 years
Package : SOP8K (200 mil)

* This product is licensed from Silicon Storage Technology, Inc. (USA).

ORDERING INFORMATION
See detailed ordering and shipping information on page 21 of this data sheet.

Package Dimensions

unit : mm

SOIC-8 / SOP8K (200 mil)
CASE 751CV
ISSUE O

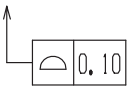
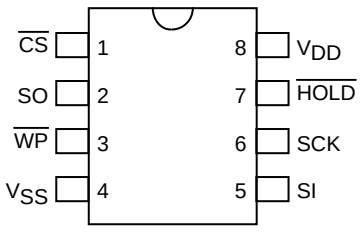


Figure 1 Pin Assignments



Top view

Figure 2 Block Diagram

Table 1 Pin Description

Symbol	Pin Name	Description
SCK	Serial clock	This pin controls the data input/output timing. The input data and addresses are latched synchronized to the rising edge of the serial clock, and the data is output synchronized to the falling edge of the serial clock.
SI	Serial data input	The data and addresses are input from this pin, and latched internally synchronized to the rising edge of the serial clock.
SO	Serial data output	The data stored inside the device is output from this pin synchronized to the falling edge of the serial clock.
$\overline{CS}$	Chip select	The device becomes active when the logic level of this pin is low; it is deselected and placed in standby status when the logic level of the pin is high.
$\overline{WP}$	Write protect	The status register wr

Device Operation

The LE25U20AMB features electrical on-chip erase functions using a single 2.5 V power supply, that have been added to the EPROM functions of the industry standard that support serial interfaces. Interfacing and control are facilitated by incorporating the command registers inside the chip. The read, erase, program and other required functions of the device are executed through the command registers. The command addresses and data input in accordance with "Table 2 Command Settings" are latched inside the device in order to execute the required operations. "Figure 3 Serial Input Timing" shows the timing waveforms of the serial data input. First, at the falling $\overline{CS}$ edge the device is selected, and serial input is enabled for the commands, addresses, etc. These inputs are introduced internally in sequence starting with bit 7 in synchronization with the rising SCK edge. At this time, output pin SO is in the high-impedance state. The output pin is placed in the low-impedance state when the data is output in sequence starting with bit 7 synchronized to the falling clock edge during read, status register read and silicon ID. Refer to "Figure 4 Serial Output Timing" for the serial output timing.

The LE25U20AMB supports both serial interface SPI mode 0 and SPI mode 3. At the falling $\overline{CS}$ edge, SPI mode 0 is automatically selected if the logic level of SCK is low, and SPI mode 3 is automatically selected if the logic level of SCK is high.

Table 2 Command Settings

Command	1st bus cycle	2nd bus cycle	3rd bus cycle	4th bus cycle	5th bus cycle	6th bus cycle	Nth bus cycle
Read	03h	A23-A16	A15-A8	A7-A0			
	0Bh	A23-A16	A15-A8	A7-A0	X		
Small sector erase	D7h/20h	A23-A16	A15-A8	A7-A0			
Sector erase	D8h	A23-A16	A15-A8	A7-A0			
Chip erase	C7h						
Page program	02h	A23-A16	A15-A8	A7-A0	PD *	PD *	PD *
Write enable	06h						

Figure 3 Serial Input Timing

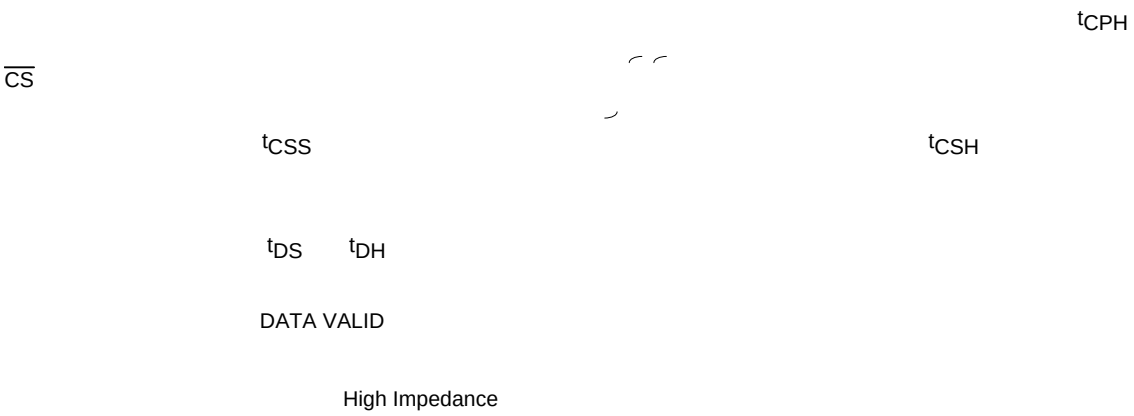


Figure 4 Serial Output Timing

Description of Commands and Their Operations

"Table 2 Command Settings" provides a list and overview of the commands. A detailed description of the functions and operations corresponding to each command is presented below.

1. Read

There are two read commands, the 4 bus cycle read command and 5 bus cycle read command. Consisting of the first through fourth bus cycles, the 4 bus cycle read command inputs the 24-bit addresses following (03h), and the data in the designated addresses is output synchronized to SCK. The data is output from SO on the falling clock edge of fourth bus cycle bit 0 as a reference. "Figure 5-a 4 Bus Read" shows the timing waveforms.

Consisting of the first through fifth bus cycles, the 5 bus cycle read command inputs the 24-bit addresses and 8 dummy bits following (0Bh). The data is output from SO using the falling clock edge of fifth bus cycle bit 0 as a reference. "Figure 5-b 5 Bus Read" shows the timing waveforms. The only difference between these two commands is whether the dummy bits in the fifth bus cycle are input.

2. Status Registers

The status registers hold the operating and setting statuses inside the device, and this information can be read (status register read) and the protect information can be rewritten (status register write). There are 8 bits in total, and "Table 3 Status registers" gives the significance of each bit.

Table 3 Status Registers

Bit	Name	Logic	Function	Power-on Time Information

2-2. Status Register Write

The information in status registers BP0, BP1, and SRWP can be rewritten using the status register write command. RDY, WEN, bit 4, bit 5, and bit 6 are read-only bits and cannot be rewritten. The information in bits BP0, BP1, and SRWP is stored in the non-volatile memory, and when it is written in these bits, the contents are retained even at power-down. "Figure 7 Status Register Write" shows the timing waveforms of status register write, and Figure 20 shows a status register write flowchart. Consisting of the first and second bus cycles, the status register write command initiates the internal write operation at the rising CS edge after the data has been input following (01h). Erase and program are performed automati

WEN (bit 1)

The WEN register is for detecting whether the device can perform write operations. If it is set to "0", the device will not perform the write operation even if the write command is input. If it is set to "1", the device can perform write operations in any area that is not block-protected.

WEN can be controlled using the write enable and write disable commands. By inputting the write enable command (06h), WEN can be set to "1"; by inputting the write disable command (04h), it can be set to "0". In the following states, WEN is automatically set to "0" in order to protect against unintentional writing.

At power-on

Upon completion of small sector erase, sector erase or chip erase

Upon completion of page program

Upon completion of status register write

* If a write operation has not been performed inside the LE25U20AMB because, for instance, the command input for any of the write operations (small sector erase, sector erase, chip erase, page program, or status register write) has failed or a write operation has been performed for a protected address, WEN will retain the status established prior to the issue of the command concerned. Furthermore, its state will not be changed by a read operation.

BP0, BP1 (bits 2, 3)

Block protect BP0 and BP1 are status register bits that can be rewritten, and the memory space to be protected can be set depending on these bits. For the setting conditions, refer to "Table 4 Protect level setting conditions".

Table 4 Protect Level Setting Conditions

Protect Level	Status Register Bits	Protected Area

3. Write Enable

Before performing any of the operations listed below, the device must be placed in the write enable state. Operation is the same as for setting status register WEN to "1", and the state is enabled by inputting the write enable command. "Figure 8 Write Enable" shows the timing waveforms when the write enable operation is performed. The write enable command consists only of the first bus cycle, and it is initiated by inputting (06h).

Small sector erase, sector erase, chip erase
Page program
Status register write

4. Write Disable

The write disable command sets status register WEN to "0" to prohibit unintentional writing. "Figure 9 Write Disable" shows the timing waveforms. The write disable command consists only of the first bus cycle, and it is initiated by inputting (04h). The write disable state (WEN "0") is exited by setting WEN to "1" using the write enable command (06h).

Figure 8 Write Enable

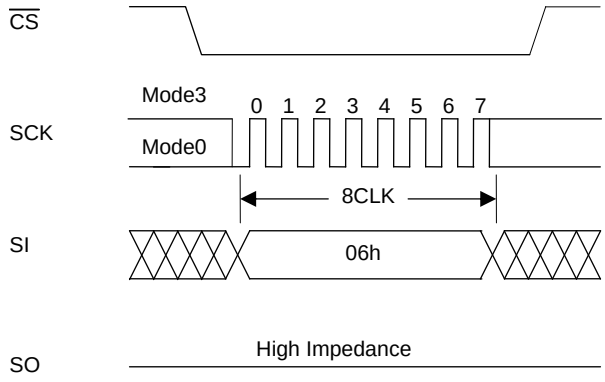
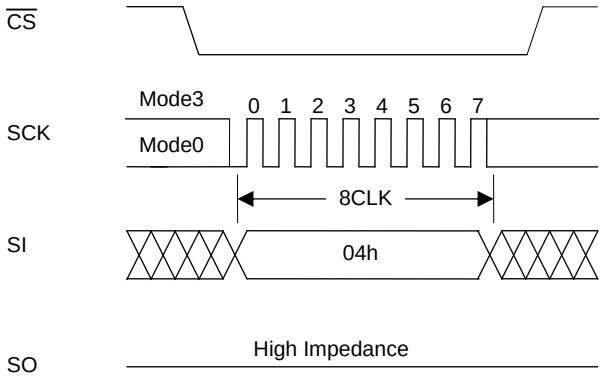


Figure 9 Write Disable



5. Power-down

The power-down command sets all the commands, with the exception of the silicon ID read command and the command to exit from power-down, to the acceptance prohibited state (power-down). "Figure 10 Power-down" shows the timing waveforms. The power-down command consists only of the first bus cycle, and it is initiated by inputting (B9h). However, a power-down command issued during an internal write operation will be ignored. The power-down state is exited using the power-down exit command (power-down is exited also when one bus cycle or more of the silicon ID read command (ABh) has been input). "Figure 11 Exiting from Power-down" shows the timing waveforms of the power-down exit command.

Figure 10 Power-down

Figure 11 Exiting from Power-down

8. Chip Erase

Chip erase is an operation that sets the memory cell data in all the sectors to "1". "Figure 14 Chip Erase" shows the timing waveforms, and Figure 21 shows a chip erase flowchart. The chip erase command consists only of the first bus cycle, and it is initiated by inputting (C7h). After the command has been input, the internal erase operation starts from the rising $\overline{CS}$ edge, and it ends automatically by the control exercised by the internal timer. Erase end can also be detected using status register $\overline{RDY}$.

Figure 14 Chip Erase

9. Page Program

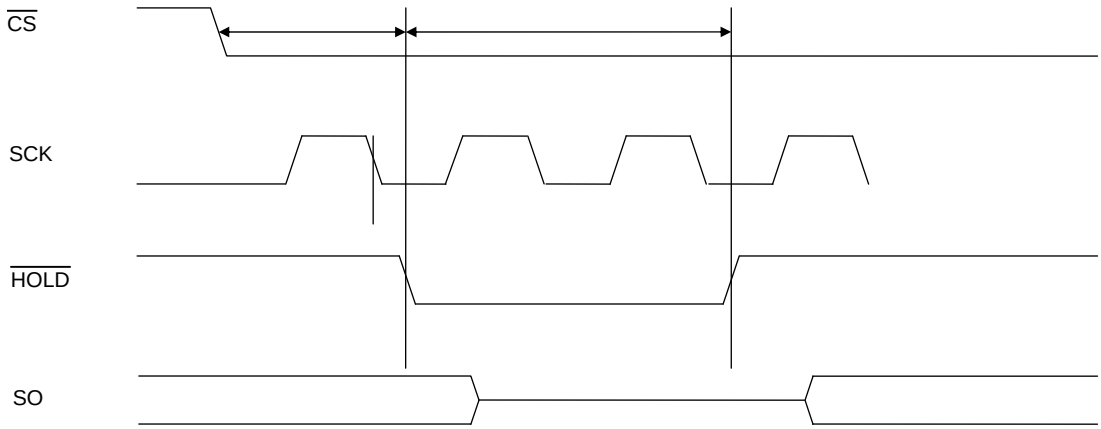
Page program is an operation that programs any number of bytes from 1 to 256 bytes within the same sector page (page addresses: A17 to A8). Before initiating page program, the data on the page concerned must be erased using small sector erase, sector erase, or chip erase. "Figure 15 Page Program" shows the page program timing waveforms, and Figure 22 shows a page program flowchart. After the falling $\overline{CS}$

10. Silicon ID Read

11. Hold Function

Using the $\overline{HOLD}$ pin, the hold function suspends serial communication (it places it in the hold status). "Figure 17 $\overline{HOLD}$" shows the timing waveforms. The device is placed in the hold status at the falling $\overline{HOLD}$ edge while the logic level of SCK is low, and it exits from the hold status at the rising $\overline{HOLD}$ edge. When the logic level of SCK is high, $\overline{HOLD}$ must not rise or fall. The hold function takes effect when the logic level of $\overline{CS}$ is low, the hold status is exited and serial communication is reset at the rising $\overline{CS}$ edge. In the hold status, the SO output is in the high-impedance state, and SI and SCK are "don't care".

Figure 17 $\overline{HOLD}$



12. Power-on

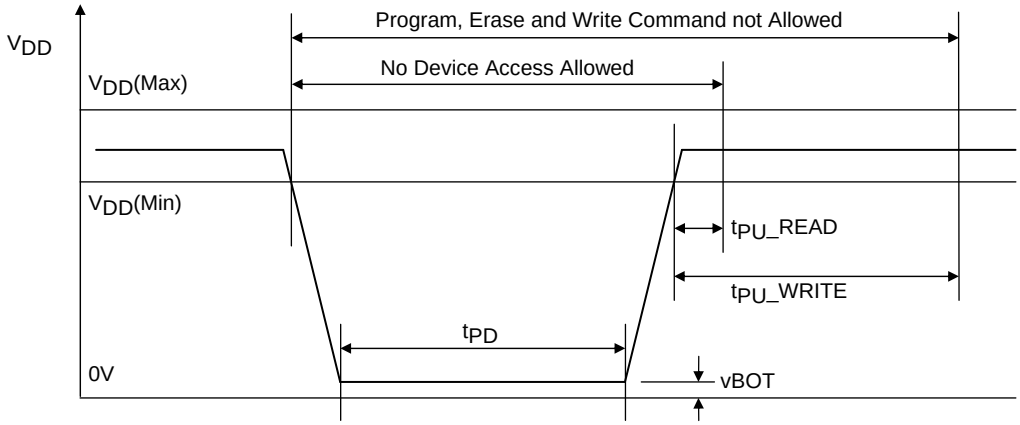
In order to protect against unintentional writing, $\overline{CS}$ must be kept at V_{CC} At power-on. After power-on, the supply voltage has stabilized at 2.30 V or higher, wait for 100 s (t_{PU_READ}) before inputting the command to start a read operation. Similarly, wait for 10ms (t_{PU_WRITE}) after the voltage has stabilized before inputting the command to start a write operation.

Figure 18 Power-on Timing

13. Hardware Data Protection

In order to protect against unintentional writing at power-on, the LE25U20AMB incorporates a power-on reset function. The following conditions must be met in order to ensure that the power reset circuit will operate stably.
No guarantees are given for data in the event of an instantaneous power failure occurring during the writing period.

Figure 19 Power-down Timing



14. Software Data Protection

The LE25U20AMB eliminates the possibility of unintentional operations by not recognizing commands under the following conditions.

When a write command is input and the rising $\overline{CS}$ edge timing is not in a bus cycle (8 CLK units of SCK)
When the page program data is not in 1-byte increments
When the status register write command is input for 2 bus cycles or more

15. Decoupling Capacitor

A 0.1 F ceramic capacitor must be provided to each device and connected between V_{DD} and V_{SS} in order to ensure that the device will operate stably.

Specifications

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Ratings	unit
Maximum supply voltage	V_{DD} max	With respect to V_{SS}	0.5 to +4.6	V
DC voltage (all pins)	VIN/VOUT	With respect to V_{SS}	0.5 to V_{DD}+0.5	V
Storage temperature	Tstg		55 to +150	C

Operating Conditions

Parameter	Symbol	Conditions	Ratings	unit
Operating supply voltage	V_{DD}		2.30 to 3.60	V
Operating ambient temperature	Topr		40 to +85	C

Allowable DC Operating Conditions

Parameter	Symbol	Conditions	Ratings			unit
			min	typ	max	
Read mode operating current	I_{CCR}	$\overline{CS}$ = 0.1V_{DD}, $\overline{HOLD}$ = $\overline{WP}$ = 0.9V_{DD} SI = 0.1V_{DD} / 0.9V_{DD}, SO = open operating frequency = 30 MHz, V_{DD} = V_{DD} max			6	mA
Write mode operating current (erase+page program)	I_{CCW}	V_{DD} = V_{DD} max,9984312.7(0)12e54T28 Tw68 -.w1c 0 Tw(1.4j1.4359 .28212 TD.00628 Tc.=ng cu 049mTw(s,5(en)9				

AC Characteristics

Parameter	Symbol	Ratings			unit
		min	typ	max	
Clock frequency	f_{CLK}			30	MHz
SCK logic high level pulse width	t_{CLHI}	16			ns
SCK logic low level pulse width	t_{CLLO}	16			ns
Input signal rising/falling time	t_{RF}			20	ns
$\overline{CS}$ setup time	t_{CSS}	10			ns
$\overline{CS}$ hold time	t_{CSH}	10			ns
Data setup time	t_{DS}	5			ns
Data hold time	t_{DH}	5			ns
$\overline{CS}$ wait pulse width	t_{CPH}	25			ns
Output high impedance time from $\overline{CS}$	t_{CHZ}			15	ns
Output data time from SCK	t_V		10	15	ns
Output data hold time	t_{HO}	1			ns
$\overline{HOLD}$ setup time	t_{HS}	7			ns
$\overline{HOLD}$ hold time	t_{HH}	3			ns
Output low impedance time from $\overline{HOLD}$	t_{HLZ}				

Figure 20 Status Register Write Flowchart

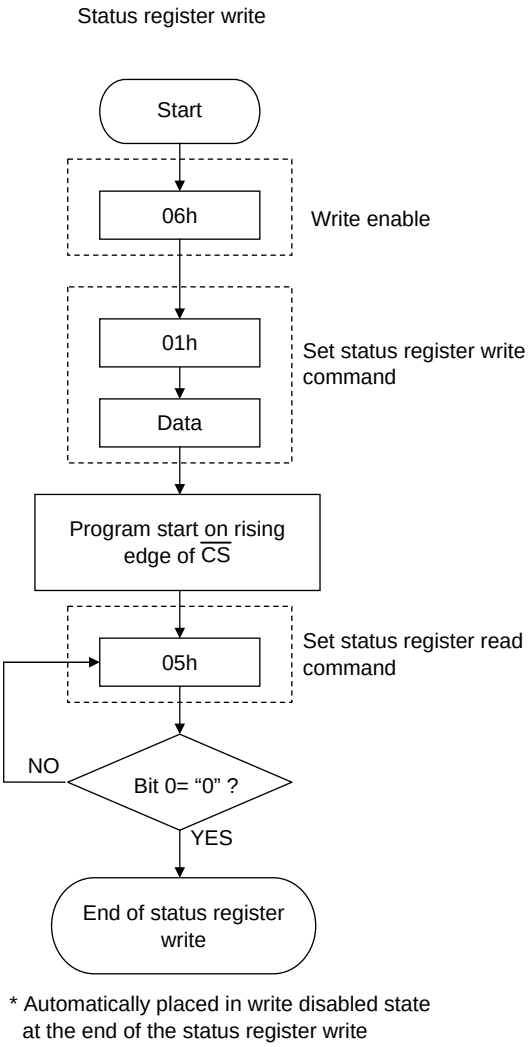


Figure 21 Erase Flowcharts

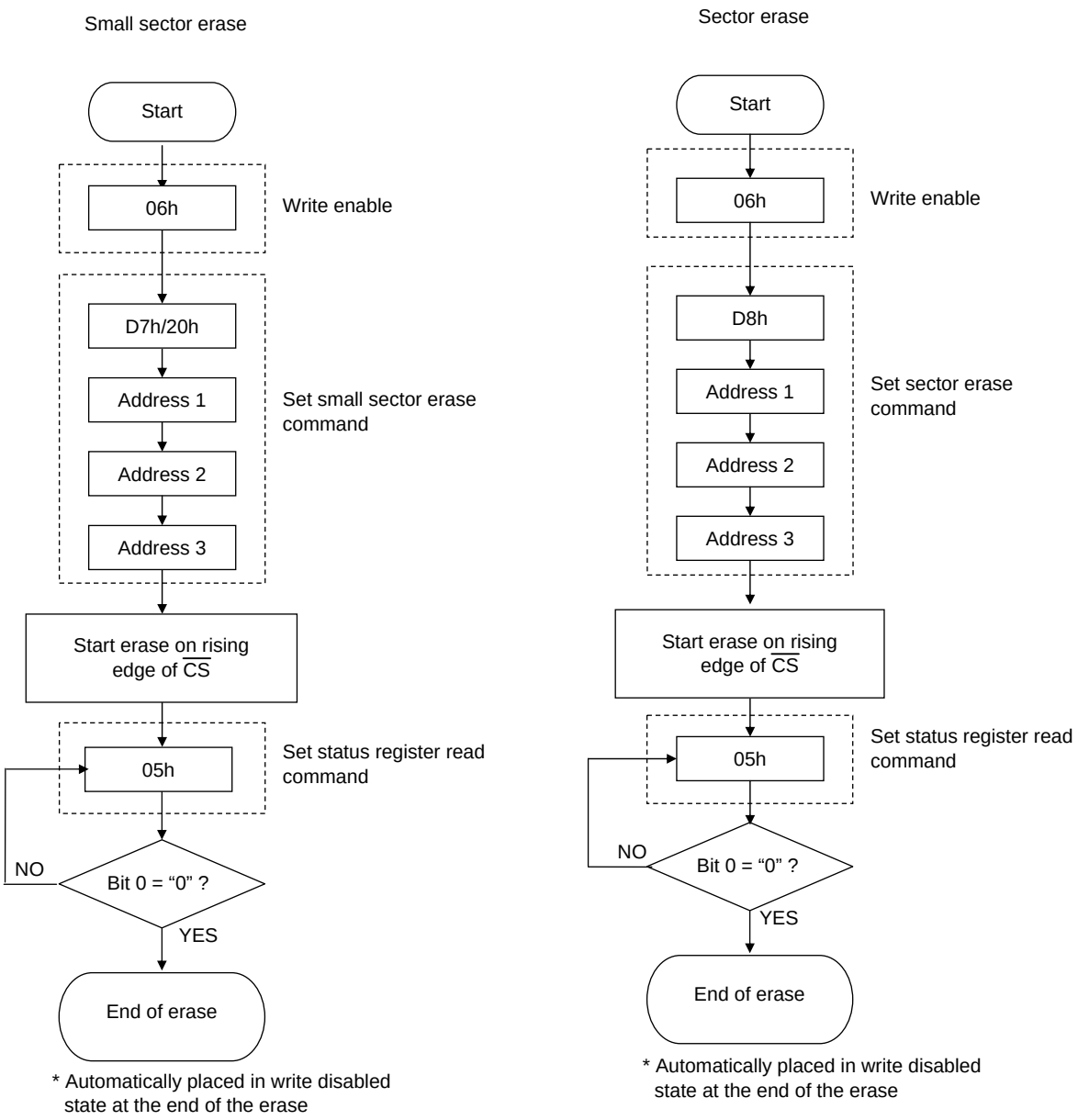


Figure 22 Page Program Flowchart