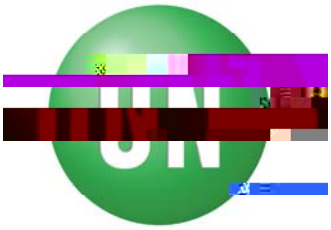

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ORDERING INFORMATION

See detailed ordering and shipping information on page 23 of this data sheet.

Package Dimensions

unit : mm

SOIC-8 / SOP8J (200 mil)
CASE 751CU
ISSUE O

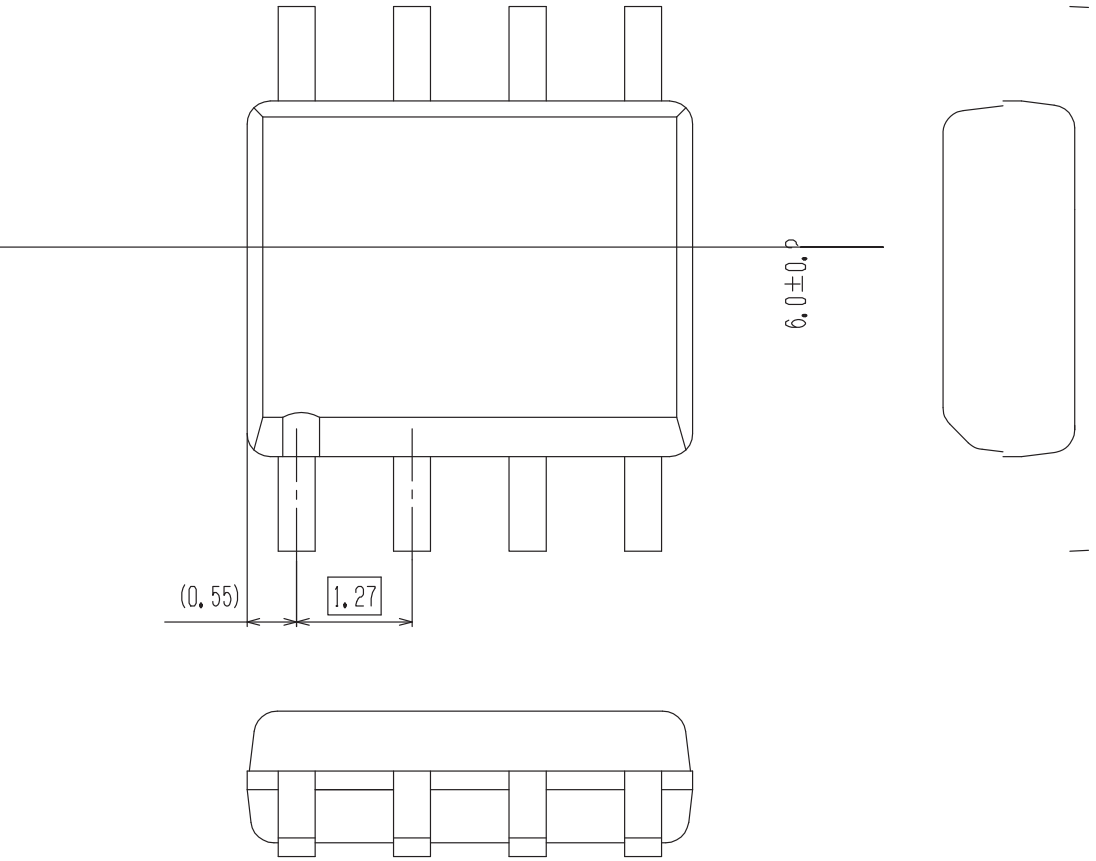
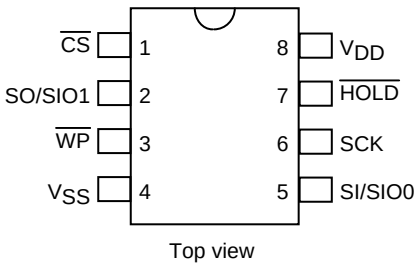


Figure 1 Pin Assignments



Top view

Figure 2 Block Diagram

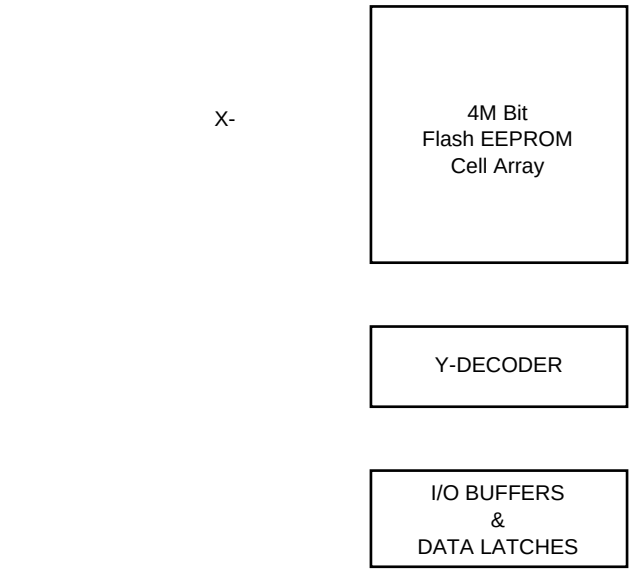


Table 1 Pin Description

Symbol	Pin Name	Description
SCK	Serial clock	This pin controls the data input/output timing. The input data and addresses are latched synchronized to the rising edge of the serial clock, and the data is output synchronized to the falling edge of the serial clock.
SI/SIO0	Serial data input / Serial data input output	The data and addresses are input from this pin, and latched internally synchronized to the rising edge of the serial clock. It changes into the output pin at Dual Output and it changes into the input output pin at Dual I/O.
SO/SIO1	Serial data input / Serial data input output	The data stored inside the device is output from this pin synchronized to the falling edge of the serial clock. It changes into the output pin at Dual Output and it changes into the input output pin at Dual I/O.
$\overline{CS}$	Chip select	The device becomes active when the logic level of this pin is low; it is deselected and placed in standby status when the logic level of the pin is high.
$\overline{WP}$	Write protect	The status register write protect (SRWP) takes effect when the logic level of this pin is low.
$\overline{HOLD}$	Hold	Serial communication is suspended when the logic level of this pin is low.
V_{DD}	Power supply	This pin supplies the 2.3 to 3.6 V supply voltage.
V_{SS}	Ground	This pin supplies the 0 V supply voltage.

Device Operation

The read, erase, program and other required functions of the device are executed through the command registers. The serial I/O corrugate is shown in Figure 3 and the command list is shown in Table 2. At the falling $\overline{CS}$ edge the device is selected, and serial input is enabled for the commands, addresses, etc. These inputs are normalized in 8 bit units and taken into the device interior in synchronization with the rising edge of SCK, which causes the device to execute operation according to the command that is input.

The LE25U40PCMC supports both serial interface SPI mode 0 and SPI mode 3. At the falling $\overline{CS}$ edge, SPI mode 0 is automatically selected if the logic level of SCK is low, and SPI mode 3 is automatically selected if the logic level of SCK is high.

Figure 3 I/O waveforms

Table 2 Command Settings

Command	1st bus cycle	2nd bus cycle	3rd bus cycle	4th bus cycle	5th bus cycle	6th bus cycle	Nth bus cycle
Read	03h	A23-A16	A15-A8	A7-A0	RD *1	RD *1	RD *1
High Speed Read	0Bh	A23-A16	A15-A8	A7-A0	X	RD *1	RD *1
Dual Read	3Bh	A23-A16	A15-A8	A7-A0	Z	RD *1	RD *1
Dual I/O Read	BBh	A23-A8	A7-A0,X, Z	RD *1	RD *1	RD *1	RD *1
Small sector erase	20h / D7h	A23-A16	A15-A8	A7-A0			
Sector erase	D8h	A23-A16	A15-A8	A7-A0			
Chip erase	60h / C7h						
Page program	02h	A23-A16	A15-A8	A7-A0	PD *2	PD *2	PD *2
Write enable	06h						
Write disable	04h						
Power down	B9h						
Status register read	05h						
Status register write	01h	DATA					
JEDEC ID read	9Fh						
ID read	ABh	X	X	X			

Table 3 Command Settings

4M bit

Description of Commands and Their Operations

A detailed description of the functions and operations corresponding to each command is presented below.

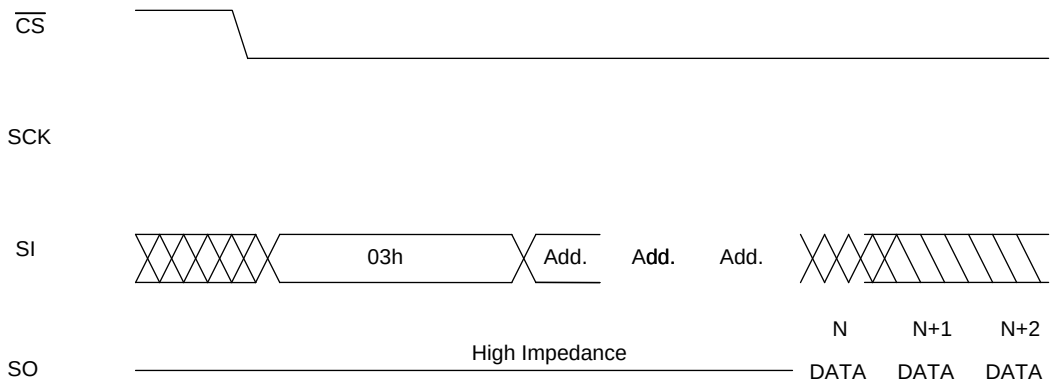
1. Standard SPI read

There are two read commands, the standard SPI read command and High-speed read command.

1-1. Read command

Consisting of the first through fourth bus cycles, the 4 bus cycle read command inputs the 24-bit addresses following (03h). The data is output from SO on the falling clock edge of fourth bus cycle bit 0 as a reference. "Figure 4-a Read" shows the timing waveforms.

Figure 4-a Read



1-2. High-speed Read command

Consisting of the first through fifth bus cycles, the High-speed read command inputs the 24-bit addresses and 8 dummy bits following (0Bh). The data is output from SO using the falling clock edge of fifth bus cycle bit 0 as a reference. "Figure 4-b High-speed Read" shows the timing waveforms.

Figure 4-b High-speed Read

2. Dual read

There are two Dual read commands, the Dual read command and the Dual I/O read command. They achieve the twice speed-up from a High-speed read command.

2-1. Dual Read command

The Dual read command changes SI/SIO0 into the output pin function in addition to SO/SIO1, makes the data output 2 bit and has achieved a high-speed output. Consisting of the first through fifth bus cycles, the Dual read command inputs the 24-bit addresses and 8 dummy bits following (3Bh). DATA1 (Bit7, BIt5, Bit3 and Bit1) is output from SI/SIO0 and DATA0 (Bit6, Bit4, Bit2 and Bit0) is output from SO/SIO1 on the falling clock edge of fifth bus cycle bit 0 as a reference. "Figure 5-a Dual Read" shows the timing waveforms.

Figure 5-a Dual Read

2-2. Dual I/O Read command

The Dual I/O read command changes SI/SIO0 and SO/SIO1 into the input output pin function, makes the data input and output

3. Status Registers

The status registers hold the operating and setting statuses inside the device, and this information can be read (status register read) and the protect information can be rewritten (status register write). There are 8 bits in total, and "Table 4 Status registers" gives the significance of each bit.

Table 4 Status Registers

Bit	Name	Logic	Function	Power-on Time Information
Bit0	$\overline{\text{RDY}}$	0	Ready	0
		1	Erase/Program	
Bit1	WEN	0	Write disabled	0
		1	Write enabled	
Bit2	BP0	0	Block protect information Protecting area switch	Nonvolatile information
		1		
Bit3	BP1	0		Nonvolatile information
		1		
Bit4	BP2	0		Nonvolatile information
		1		
Bit5	TB	0	Block protect Upper side/Lower side switch	Nonvolatile information
		1		

3-2. Status register write

The information in status registers BP0, BP1, BP2, TB and SRWP can be rewritten using the status register write command. $\overline{\text{RDY}}$, WEN and bit 6 are read-only bits and cannot be rewritten. The information in bits BP0, BP1, BP2, TB and SRWP is stored in the non-volatile memory, and when it is written in these bits, the contents are retained

BP0, BP1, BP2, TB (Bits 2, 3, 4, 5)

Block protect BP0, BP1, BP2 and TB are status register bits that can be rewritten, and the memory space to be protected can be set depending on these bits. For the setting conditions, refer to "Table 5 Protect level setting conditions".

BP0, BP1, and BP2 are used to select the protected area and TB to allocate the protected area to the higher-order address area or lower-order address area.

Table 5 Protect Level Setting Conditions

Protect Level	Status Register Bits				Protected Area
	TB	BP2	BP1	BP0	
0 (Whole area unprotected)	X	0	0	0	None
T1 (Upper side 1/8 protected)	0	0	0	1	07FFFFh to 070000h
T2 (Upper side 1/4 protected)	0	0	1	0	07FFFFh to 060000h
T3 (Upper side 1/2 protected)	0	0	1	1	07FFFFh to 040000h
B1 (Lower side 1/8 protected)	1	1	0	1	00FFFFh to 000000h
B2 (Lower side 1/4 protected)	1	1	1	0	01FFFFh to 000000h
B3 (Lower side 1/2 protected)	1	1	1	1	03FFFFh to 000000h
4 (Whole area protected)	X	1	X	X	07FFFFh to 000000h

* Chip erase is enabled only when the protect level is 0.

SRWP (bit 7)

Status register write protect SRWP is the bit for protecting the status registers, and its information can be rewritten. When SRWP is "1" and the logic level of the $\overline{WP}$ pin is low, the status register write command is ignored, and status registers BP0, BP1, BP2, TB and SRWP are protected. When the logic level of the $\overline{WP}$ pin is high, the status registers are not protected regardless of the SRWP state. The SRWP setting conditions are shown in "Table 6 SRWP setting conditions".

Table 6 SRWP Setting Conditions

$\overline{WP}$ Pin	SRWP	Status Register Protect State
0	0	Unprotected
	1	Protected
1	0	Unprotected
	1	Unprotected

Bit 6 are reserved bits, and have no significance.

4. Write Enable

Before performing any of the operations listed below, the device must be placed in the write enable state. Operation is the same as for setting status register WEN to "1", and the state is enabled by inputting the write enable command. "Figure 8 Write Enable" shows the timing waveforms when the write enable operation is performed. The write enable command consists only of the first bus cycle, and it is initiated by inputting (06h).

Small sector erase, sector erase, chip erase
Page program
Status register write

5. Write Disable

The write disable command sets status register WEN to "0" to prohibit unintentional writing. "Figure 9 Write Disable" shows the timing waveforms. The write disable command consists only of the first bus cycle, and it is initiated by inputting (04h). The write disable state (WEN "0") is exited by setting WEN to "1" using the write enable command (06h).

Figure 8 Write Enable

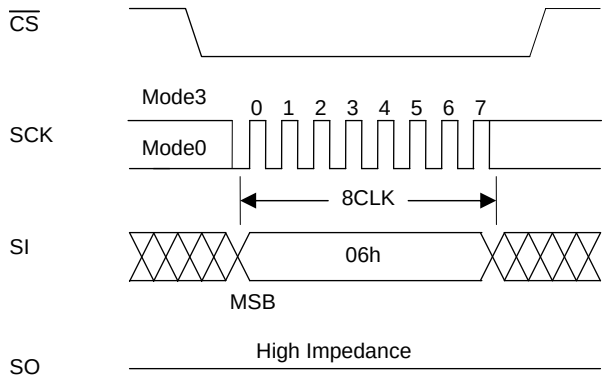
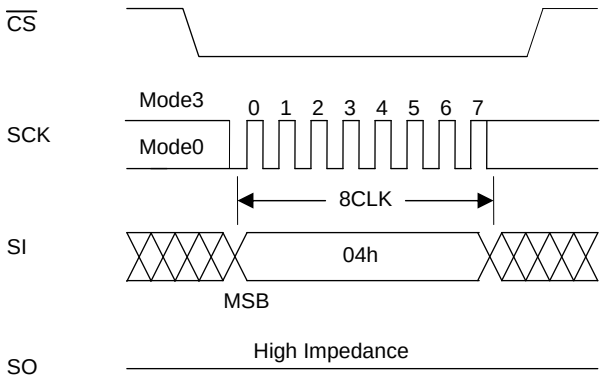


Figure 9 Write Disable



6. Power-down

The power-down command sets all the commands, with the exception of the silicon ID read command and the command to exit from power-down, to the acceptance prohibited state (power-down). "Figure 10 Power-down" shows the timing waveforms. The power-down command consists only of the first bus cycle, and it is initiated by inputting (B9h). However, a power-down command issued during an internal write operation will be ignored. The power-down state is exited using the power-down exit command (power-down is exited also when one bus cycle or more of the silicon ID read command (ABh) has been input). "Figure 11 Exiting from Power-down" shows the timing waveforms of the power-down exit command.

Figure 10 Power-down

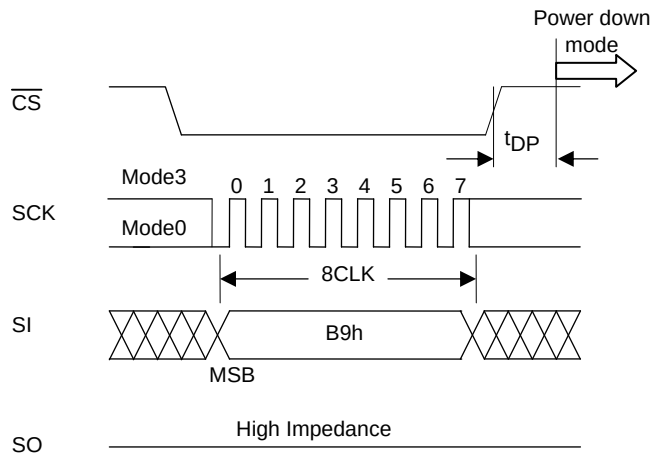
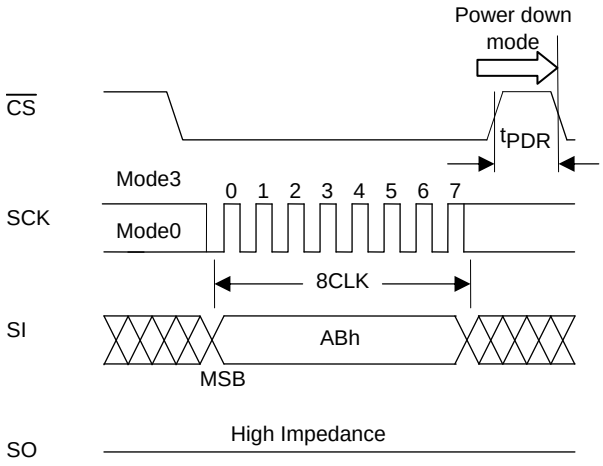


Figure 11 Exiting from Power-down



7. Small Sector Erase

Small sector erase is an operation that sets the memory cell data in any small sector to "1". A small sector consists of

9. Chip Erase

Chip erase is an operation that sets the memory cell data in all the sectors to "1". "Figure 14 Chip Erase" shows the timing waveforms, and Figure 21 shows a chip erase flowchart. The chip erase command consists only of the first bus cycle, and it is initiated by inputting (60h) or (C7h). After the command has been input, the internal erase operation starts from the rising $\overline{CS}$ edge, and it ends automatically by the control exercised by the internal timer. Erase end can also be detected using status register $\overline{RDY}$.

Figure 14 Chip Erase

10. Page Program

Page program is an operation that programs any number of

11. Silicon ID Read

ID read is an operation that reads the manufacturer code and device ID information. The silicon ID read command is not accepted during writing. There are two methods of reading the silicon ID, each of which is assigned a device ID. In the first method, the read command sequence consists only of the first bus cycle in which (9Fh) is input. In the subsequent bus cycles, the manufacturer code 62h which is assigned by JEDEC, 2-byte device ID code (memory type, memory capacity), and reserved code are output sequentially. The 4-byte code is output repeatedly as long as clock inputs are present, "Table 7-1 JEDEC ID code " lists the silicon ID codes and "Figure 16-a JEDEC ID read" shows the JEDEC ID read timing waveforms.

The second method involves inputting the ID read command. This command consists of the first through fourth bus cycles, and the one bite silicon ID can be read when 24 dummy bits are input after (ABh). "Table 7-2 ID code " lists the silicon ID codes and "Figure 16-b ID read" shows the ID read timing waveforms.

If the SCK input persists after a device code is read, that device code continues to be output. The data output is transmitted starting at the falling edge of the clock for bit 0 in the fourth bus cycle and the silicon ID read sequence is finished by setting $\overline{CS}$ high.

Table 7-1 JEDEC ID code

	Output code

Table 7-2 ID code

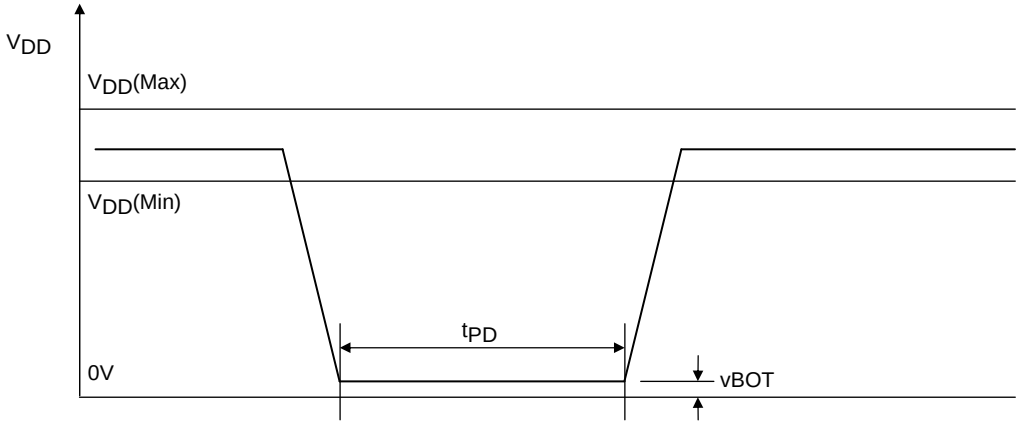
Output Code

14. Hardware Data Protection

LE25U40PCMC incorporates a power-on reset function. The following conditions must be met in order to ensure that the power reset circuit will operate stably.

No guarantees are given for data in the event of an instantaneous power failure occurring during the writing period.

Figure 19 Power-down Timing



Power-on timing

Parameter	Symbol	spec		unit
		min	max	
power-on to operation time	t_{PU}	100		µs
power-down time	t_{PD}	10		ms
power-down voltage	t_{BOT}		0.2	V

15. Software Data Protection

The LE25U40PCMC eliminates the possibility of unintentional operations by not recognizing commands under the following conditions.

When a write command is input and the rising $\overline{CS}$ edge timing is not in a bus cycle (8 CLK units of SCK)

When the page program data is not in 1-byte increments

When the status register write command is input for 2 bus cycles or more

16. Decoupling Capacitor

A 0.1 F ceramic capacitor must be provided to each device and connected between V_{DD} and V_{SS} in order to ensure that the device will operate stably.

AC Characteristics

Parameter		Symbol	Ratings			unit
			min	typ	max	
Clock frequency	Read instruction (03h)	f_{CLK}	0.01		25	MHz
	All instructions except for read (03h)		0.01		30	MHz
Input signal rising/falling time		t_{RF}	0.1			V/ns
SCK logic high level pulse width		t_{CLHI}	16			ns
SCK logic low level pulse width		t_{CLLO}	16			ns
$\overline{CS}$ setup time		t_{CSS}	10			ns
$\overline{CS}$ hold time		t_{CSH}	10			ns
Data setup time		t_{DS}				

Timing waveforms

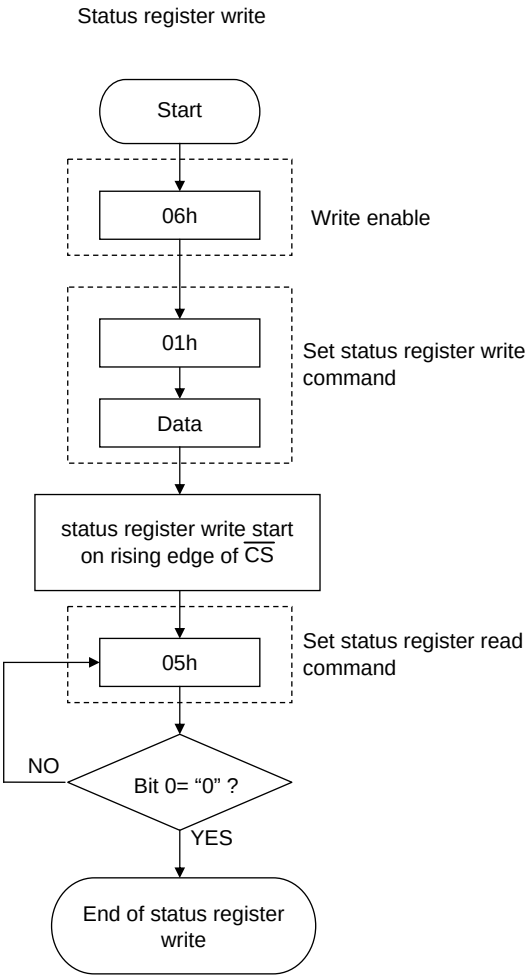
Serial Input Timing

Serial Output Timing

Hold Timing

Status resistor write Timing

Figure 20 Status Register Write Flowchart



* Automatically placed in write disabled state at the end of the status register write

Figure 22 Page Program Flowchart