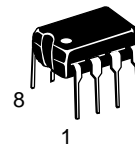




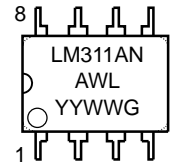
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**MARKING
DIAGRAMS**



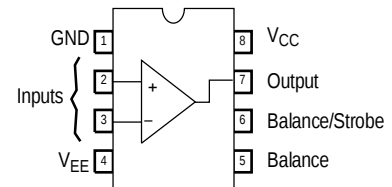
**PDIP-8
N SUFFIX
CASE 626**



**SOIC-8
D SUFFIX
CASE 751**

- x = 2 or 3
- A = Assembly Location
- WL, L = Wafer Lot
- YY, Y = Year
- WW, W = Work Week
- G = Pb-Free Package
- = Pb-Free Package

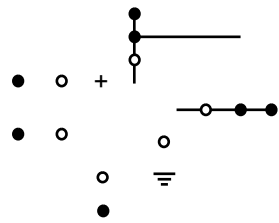
PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.



LM211, LM311

ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted) Note 1

Characteristic	Symbol	LM211			LM311			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (Note 3)	V_{IO}							

LM211, LM311

|

TECHNIQUES FOR AVOIDING OSCILLATIONS IN COMPARATOR APPLICATIONS

When a high speed comparator such as the LM211 is used with high speed input signals and low source impedances, the output response will normally be fast and stable, providing the power supplies have been bypassed (with 0.1 μ F disc capacitors), and that the output signal is routed well away from the inputs (Pins 2 and 3) and also away from Pins 5 and 6.

However, when the input signal is a voltage ramp or a slow sine wave, or if the signal source impedance is high (1.0 k Ω to 100 k Ω), the comparator may burst into oscillation near the crossing-point. This is due to the high gain and wide bandwidth of comparators like the LM211 series. To avoid oscillation or instability in such a usage, several precautions are recommended, as shown in Figure 16.

The trim pins (Pins 5 and 6) act as unwanted auxiliary inputs. If these pins are not connected to a trim-pot, they should be shorted together. If they are connected to a trim-pot, a 0.01 μ F capacitor (C1) between Pins 5 and 6 will minimize the susceptibility to AC coupling. A smaller capacitor is used if Pin 5 is used for positive feedback as in Figure 16. For the fastest response time, tie both balance pins to V_{CC} .

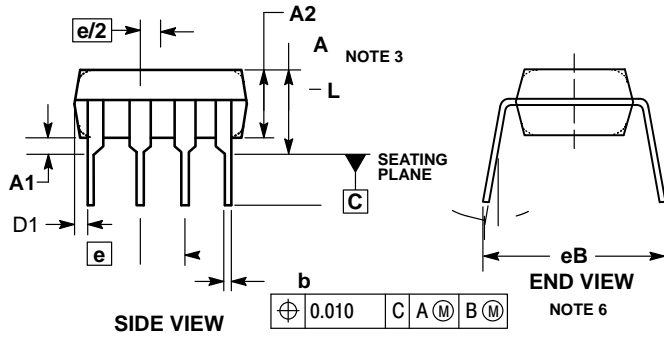
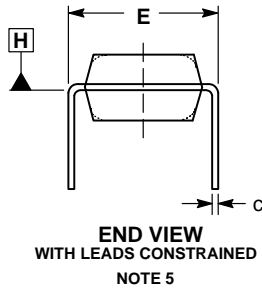
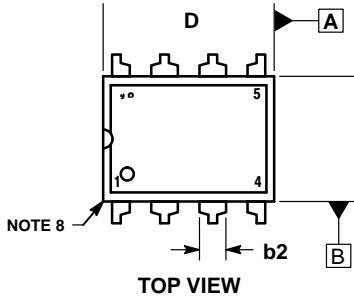
Certain sources will produce a cleaner comparator output waveform if a 100 pF to 1000 pF capacitor (C2) is connected directly across the input pins. When the signal source is applied through a resistive network, R1, it is usually advantageous to choose R2 of the same value, both for DC and for dynamic (AC) considerations. Carbon, tin-oxide, and metal-film resistors have all been used with good results in comparator input circuitry, but inductive wirewound resistors should be avoided.

When comparator circuits use input resistors (e.g., summing resistors), their value and placement are particularly important. In all cases the body of the resistor should be close to the device or socket. In other words, there should be a very short lead length or printed-circuit foil run between comparator and resistor to radiate or pick up signals. The same applies to capacitors, pots, etc. For example, if R1 = 10 k Ω , as little as 5 inches of lead between the resistors and the input pins can result in oscillations that are very hard to dampen. Twisting these input leads tightly is the best alternative to placing resistors close to the comparator.

Since feedback to almost any pin of a comparator can result in oscillation, the printed-circuit layout should be engineered thoughtfully. Preferably there should be a groundplane under the LM211 circuitry (e.g., one side of a double layer printed circuit board). Ground, positive supply or negative supply foil should extend between the output and the inputs to act as a guard. The foil connections for the inputs should be as small and compact as possible, and should not be connected to the feedback pin (Pin 1) or the output pin (Pin 7).

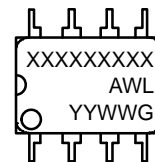
PDIP 8
CASE 626-05
ISSUE P

DATE 22 APR 2015



DIM	INCHES			
	MIN	MAX		
A	-----	0.210		
A1	0.015	-----		
A2	0.115	0.195	2.92	4.95
b	0.014	0.022		
C	0.008	0.014		
D	0.355	0.400		
D1	0.005	-----		
E	0.300	0.325		
e	0.100 BSC			
L	0.115	0.150	2.92	3.81

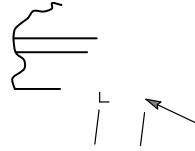
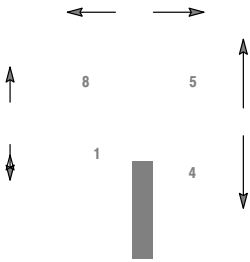
**GENERIC
MARKING DIAGRAM***



- XXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

SOIC 8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011



SEATING
PLANE



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