L`M324 , L`M2902

Α

The LM324S and LM2902S are low-cost, quad operational amplifiers with true differential inputs. They have several distinct advantages over standard operational amplifier types in single supply applications. The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.

Features

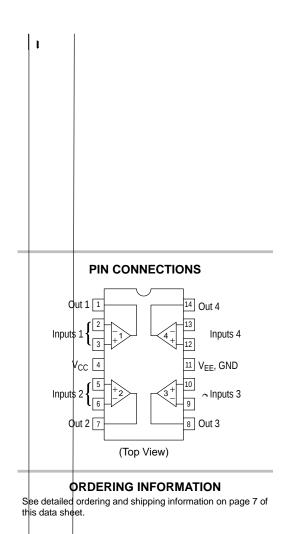
- Short Circuited Protected Outputs
- True Differential Input Stage
- Single Supply Operation: 3.0 V to 32 V
- Four Amplifiers Per Package
- Internally Compensated
- Common Mode Range Extends to Negative Supply
- Industry Standard Pinouts
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant



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MARKING DIAGRAMS



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LM324S, LM2902S

MAXIMUM RATINGS ($T_A = +25^{\circ}C$, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltages			Vdc
Single Supply	V _{CC}	32	
Split Supplies	V_{CC}, V_{EE}	±16	

LM324S, LM2902S

		LM324S		LM2902S					
Characteristics	Symbol	Min	Тур	Max	Min	Тур	Max	Unit	

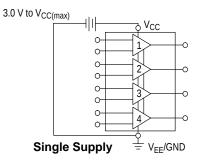
LM324S, LM2902S

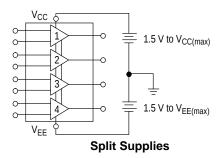
CIRCUIT DESCRIPTION

The LM324S and LM2902S are made using four internally compensated, two-stage operational amplifiers. The first stage of each consists of differential input devices Q20 and Q18 with input buffer transistors Q21 and Q17 and the differential to single ended converter Q3 and Q4. The first stage performs not only the first stage gain function but also performs the level shifting and transconductance reduction functions. By reducing the transconductance, a smaller compensation capacitor (only 5.0 pF) can be employed, thus saving chip area. The transconductance reduction is accomplished by splitting the collectors of Q20

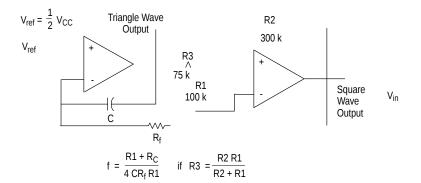
and Q18. Another feature of this input stage is that the input common mode range can include the negative supply or ground, in single supply operation, without saturating either the input devices or the differential to single–ended converter. The second stage consists of a standard current source load amplifier stage.

Each amplifier is biased from an internal-voltage regulator which has a low temperature coefficient thus giving each amplifier good temperature characteristics as well as excellent power supply rejection.









Given: f_0 = center frequency A(f_0) = gain at center frequency

Choose value f₀, C

Then: R3 =
$$\frac{Q}{f_0 C}$$

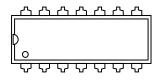
R1 = $\frac{R3}{2 A(f_0)}$
R2 = $\frac{R1 R3}{4Q^2 R1 - R3}$

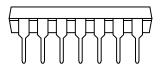
For less than 10% error from operational amplifier, $\frac{Q_0 f_0}{BW} < 0.1$

where $f_{0}\xspace$ and BW are expressed in Hz.

If source impedance varies, filter may be preceded with voltage follower buffer to stabilize filter parameters.

PDIP-





STYLE 1: PIN 1. COLLECTOR 2. BASE 3. EMITTER 4. NO CONNECTION 5. EMITTER 6. BASE 7. COLLECTOR 8. COLLECTOR 9. BASE 10. EMITTER 11. NO CONNECTION 12. EMITTER 13. BASE 14. COLLECTOR	STYLE 2: CANCELLED	STYLE 3: CANCELLED	
	STYLE 6: PIN 1. COMMON CATHODE 2. ANODE/CATHODE 3. ANODE/CATHODE 4. NO CONNECTION 5. ANODE/CATHODE 6. NO CONNECTION 7. ANODE/CATHODE 9. ANODE/CATHODE 10. NO CONNECTION 11. ANODE/CATHODE 12. ANODE/CATHODE 13. NO CONNECTION 14. COMMON ANODE	STYLE 7: PIN 1. NO CONNECTION 2. ANODE 3. ANODE 4. NO CONNECTION 5. ANODE 6. NO CONNECTION 7. ANODE 8. ANODE 9. ANODE 10. NO CONNECTION 11. ANODE 12. ANODE 13. NO CONNECTION 14. COMMON CATHODE	STYLE 8: PIN 1. NO CONNECTION 2. CATHODE 3. CATHODE 4. NO CONNECTION 5. CATHODE 6. NO CONNECTION 7. CATHODE 9. CATHODE 10. NO CONNECTION 11. CATHODE 12. CATHODE 13. NO CONNECTION 14. COMMON ANODE

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