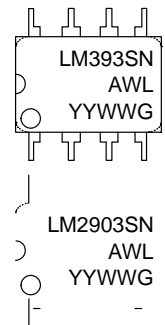




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MARKING DIAGRAMS



LMxxx = Specific Device Code
A, AL = Assembly Location
WL = Wafer Lot
Y, YY = Year
W, WW = Work Week
G or ■ = Pb-Free Package

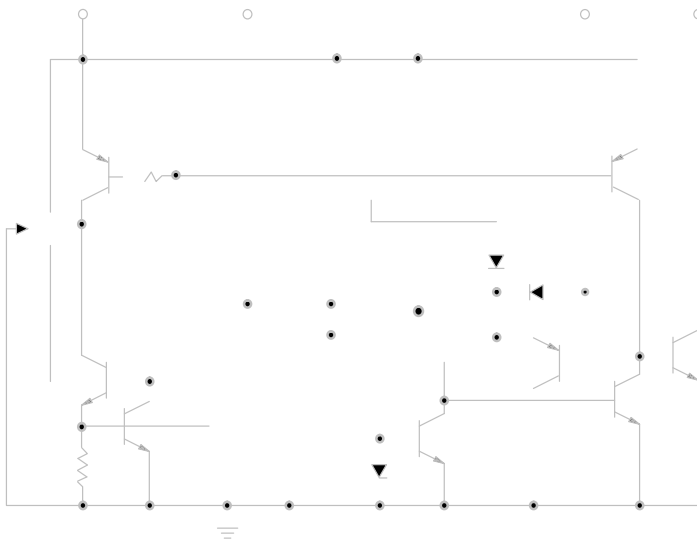
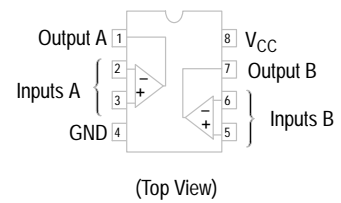


Figure 1. Representative Schematic Diagram
(Diagram shown is for 1 comparator)

PIN CONNECTIONS



ORDERING INFORMATION

See detailed marking information and ordering and shipping information on page 7 of this data sheet.

LM393S, LM2903S

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+36 or ± 18	V
Input Differential Voltage	V_{IDR}		

LM393S, LM2903S

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0 \text{ Vdc}$, $T_{low} \leq T_A \leq T_{high}$, unless otherwise noted.)

Characteristic	Symbol	LM393S			LM2903S			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (Note 3)	V_{IO}							mV
$T_A = 25^\circ\text{C}$		-	± 1.0	± 5.0	-	± 2.0	± 7.0	
$T_{low} \leq T_A \leq T_{high}$		-	-	± 9.0	-	± 9.0	± 15	
Input Offset Current	I_{IO}							nA
$T_A = 25^\circ\text{C}$		-	± 5.0	± 50	-	± 5.0	± 50	
$T_{low} \leq T_A \leq T_{high}$		-	-	± 150	-	± 50	± 200	
Input Bias Current (Note 4)	I_B							nA

LM393S, LM2903S

APPLICATIONS INFORMATION

These dual comparators feature high gain, wide bandwidth characteristics. This gives the device oscillation tendencies if the outputs are capacitively coupled to the inputs via stray capacitance. This oscillation manifests itself during output transitions (V_{OL} to V_{OH}). To alleviate this situation, input resistors $< 10\text{ k}\Omega$ should be used.

The addition of positive feedback ($< 10\text{ mV}$) is also recommended. It is good design practice to ground all unused pins.

Differential input voltages may be larger than supply voltage without damaging the comparator's inputs. Voltages more negative than -0.3 V should not be used.

D1 prevents input from going negative by more than 0.6 V.

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**Figure 2. Zero Crossing Detector
(Single Supply)**

**Figure 3. Zero Crossing Detector
(Split Supply)**

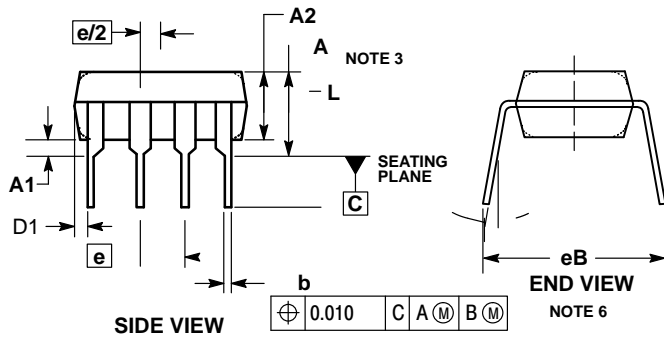
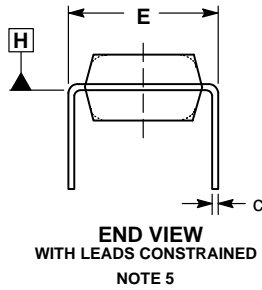
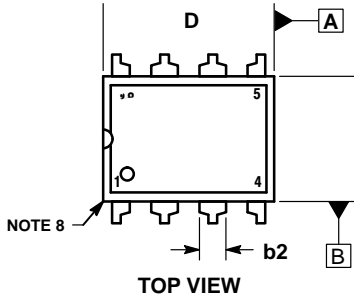
Figure 4. Free-Running Square-Wave Oscillator

Figure 5. Time Delay Generator

Figure 6. Comparator with Hysteresis

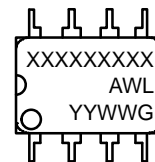
PDIP 8
CASE 626-05
ISSUE P

DATE 22 APR 2015



DIM	INCHES			
	MIN	MAX		
A	-----	0.210		
A1	0.015	-----		
A2	0.115	0.195	2.92	4.95
b	0.014	0.022		
C	0.008	0.014		
D	0.355	0.400		
D1	0.005	-----		
E	0.300	0.325		
e	0.100 BSC			
L	0.115	0.150	2.92	3.81

**GENERIC
MARKING DIAGRAM***



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