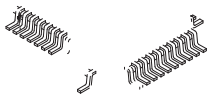
LV3313PM

Electronic Volume for Car Audio Systems

ON Semiconductor®

www.onsemi.com



PQFP44 10x10 / QIP44M

Overview

The LV3313PM is an electronic volume IC that implements a rich set of audio control functions including input selection switching function, an input gain, volume, loudness, balance, fader, and bass/treble control.

Features

Zero-cross switching circuits (Input gain control block and Volume control block) can switch signal detection location automatically.
Zero-cross switching circuits (Input gain control block and Volume control block) and soft mute circuits used for low noise even when input signals are present.
Low power consumption due to the use of BiMOS process.
All functions are controlled using serial data (CCB*).

Functions

Input selector :
Four input signals can be selected (three single-ended inputs and one differential input).
Input gain control :
The input signal can be amplified by 0 dB to +18 dB (1 dB steps).
Loudness control :
Taps are output starting at the 32 dB position of the ladder resistor and a loudness function implemented with external capacitor and resistor components.
Volume control : +10 dB to 79 dB / (1 dB steps)
L/R independent control.
Bass control : +12 dB to 12 dB in 2 dB steps
Treble control : +12 dB to 12 dB in 2 dB steps
Fader control :
The fader volume can be attenuations by one of 16 levels. Independent control each four channels. (A total of 16 settings with attenuations of 0 dB to 2 dB in 1 dB steps, 2 dB to 20 dB in 2 dB steps, and 30 dB, 45 dB, 60 dB and dB settings.)
Mute

* Computer Control Bus (CCB) is an ON Semiconductor's original bus format and the bus addresses are controlled by ON Semiconductor.

ORDERING INFORMATION

See detailed ordering and shipping information on page 19 of this data sheet.

Specifications

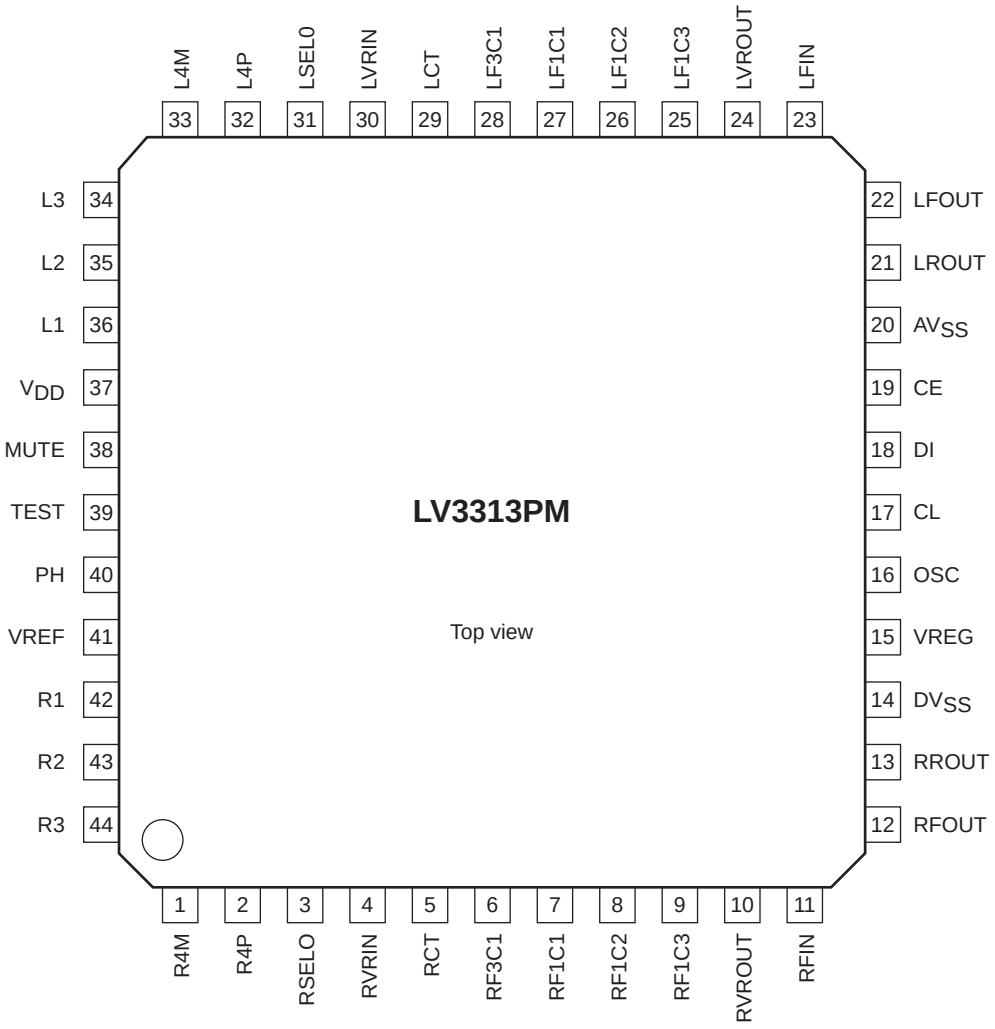
Absolute Maximum Ratings at Ta = 25 C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	V_{DD}	9.5	V
Maximum input voltage	V_{IN} max	All input pins	V_{SS} 0.3 to V_{DD}	V
Allowable power dissipation	Pd max			

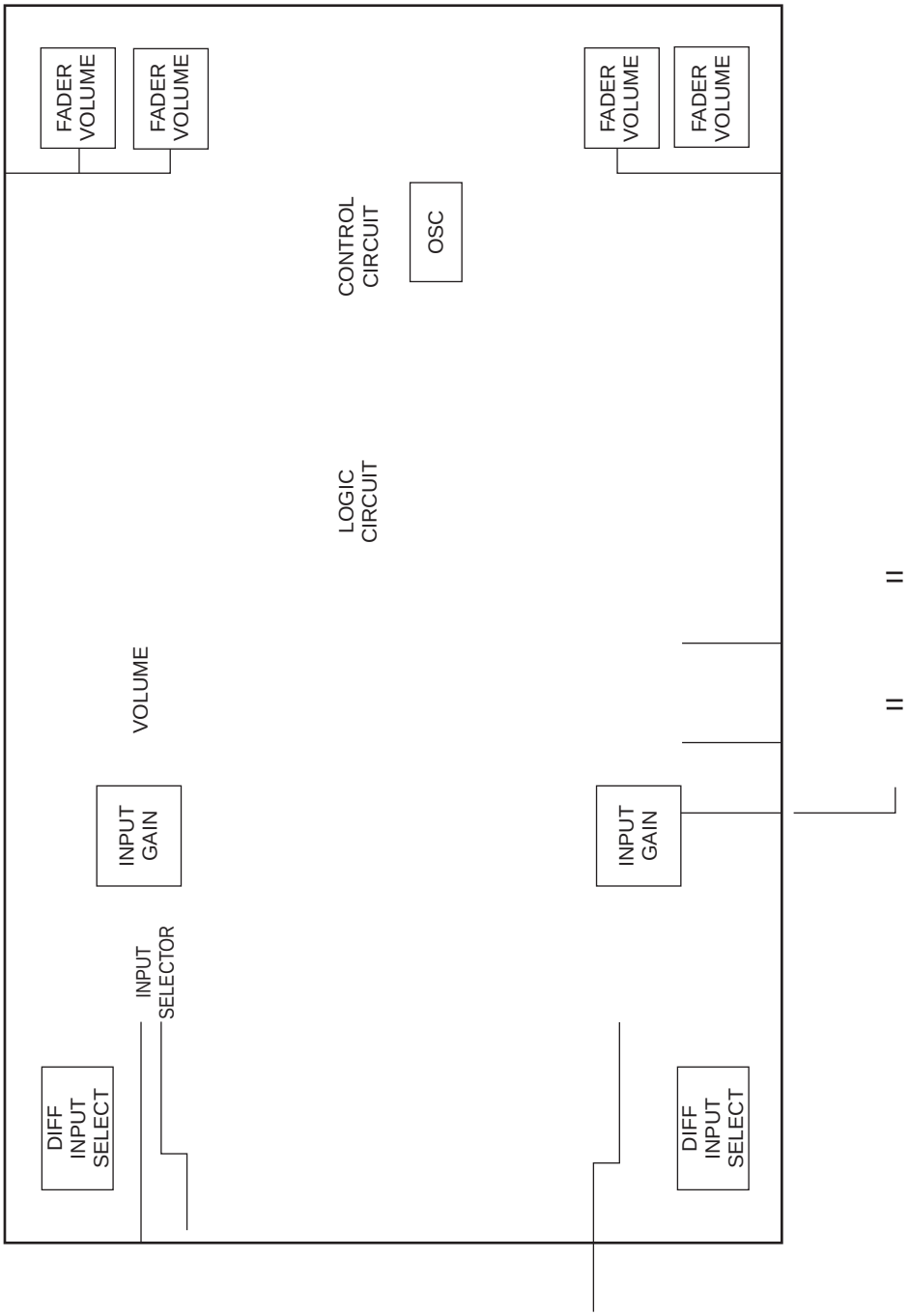
Overall Characteristics at Ta = 25°C, V_{DD} = 8 V, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
A loss of insertion	ATT		1.0		+1.0	dB
Total harmonic distortion	THD	V_{IN} = 1 Vrms, f = 1 kHz		0.004	0.01	%
Inter-input crosstalk	CT	V_{IN} = 1 Vrms, f = 1 kHz	80	88		dB
Left/Right channel crosstalk	CT	V_{IN} = 1 Vrms, f = 1 kHz	80	88		dB
Maximum attenuation	V_O min	V_{IN} = 1 Vrms, f = 1 kHz	80	88		dB
Output noise voltage	VN			10	25	V

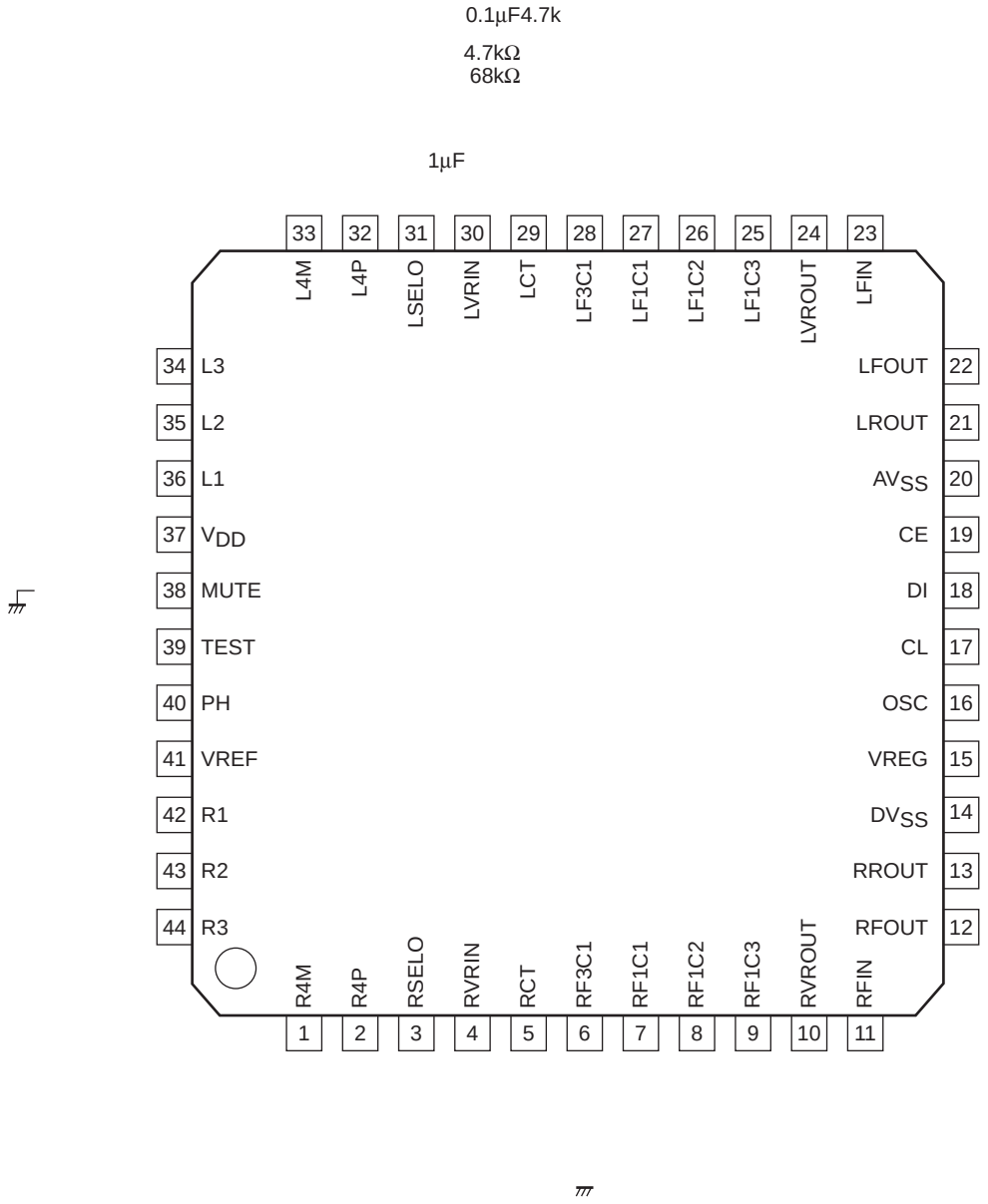
Pin Assignment



Block Diagram

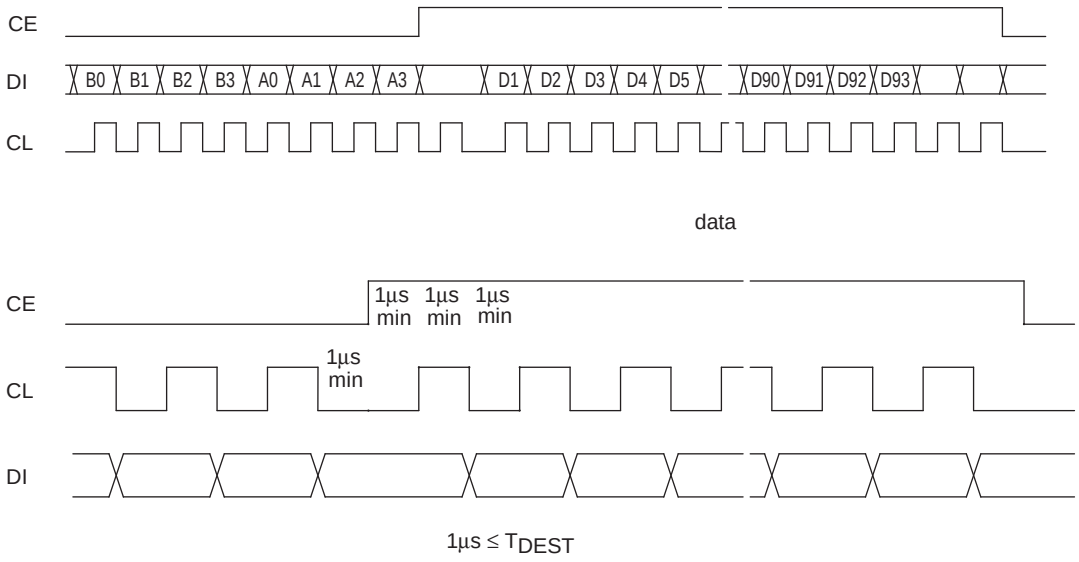


Application Circuit



Control System Timing and Data Format

The LV3313PM is controlled by applying the stipulated data to the CL, DI and CE pins. The data consists of a total of 104 bits, of which 8 bits are the device address, 96 bits are the control data.



Send to data

Address code

B0	B1	B2	B3	A0	A1	A2	A3
1	0	0	0	0	0	0	1

Data setting

Input switching control

Volume control (10 dB to 43 dB)

D13	D14	D15	D16	D17	D18	D19	D20	Lch
D21	D22	D23	D24	D25	D26	D27	D28	Rch
0	1	1	0	1	1	1	0	10dB
1	1	1	0	1	1	1	0	9dB
0	0	0	1	1	1	1	0	8dB
1	0	0	1	1	1	1	0	7dB
0	1	0	1	1	1	1	0	6dB
1	1	0	1	1	1	1	0	5dB
0	0	1	1	1	1	1	0	4dB
1	0	1	1	1	1	1	0	3dB
0	1	1	1	1	1	1	0	2dB
1	1	1	1	1	1	1	0	1dB
0	0	0	0	0	0	0	0	0dB
1	0	0	0	0	0	0	0	-1dB
0	1	0	0	0	0	0	0	-2dB
1	1	0	0	0	0	0	0	-3dB
0	0	1	0	0	0	0	0	-4dB
1	0	1	0	0	0	0	0	-5dB
0	1	1	0	0	0	0	0	-6dB
1	1	1	0	0	0	0	0	-7dB
0	0	0	1	0	0	0	0	-8dB
1	0	0	1	0	0	0	0	-9dB
0	1	0	1	0	0	0	0	-10dB
1	1	0	1	0	0	0	0	-11dB
0	0	1	1	0	0	0	0	-12dB
1	0	1	1	0	0	0	0	-13dB
0	1	1	1	0	0	0	0	-14dB
1	1	1	1	0	0	0	0	-15dB

Tone block

Treble

GAIN	D29	D30	D31	D32	Lch
	D33	D34	D35	D36	Rch
	0	1	1	1	+12dB
	1	0	1	1	+10dB
	0	0	1	1	+8dB
	1	1	0	1	+6dB
	0	1	0	1	+4dB
	1	0	0	1	+2dB
	0	0	0	0	0dB
	1	0	0	0	-2dB
	0	1	0	0	-4dB
	1	1	0	0	-6dB
	0	0	1	0	-8dB
	1	0	1	0	-10dB
	0	1	1	0	-12dB

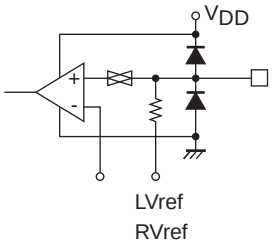
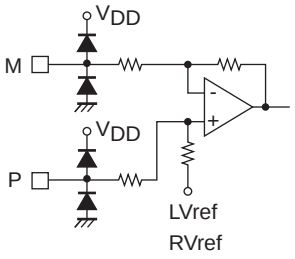
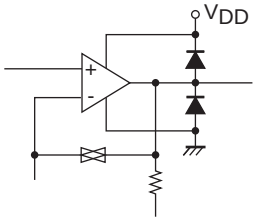
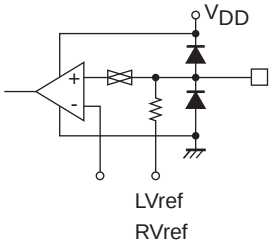
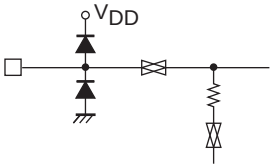
Bass

GAIN	D37	D38	D39	D40	Lch
	D41	D42	D43	D44	Rch
	0	1	1	1	+12dB
	1	0	1	1	+10dB
	0	0	1	1	+8dB
	1	1	0	1	+6dB
	0	1	0	1	+4dB
	1	0	0	1	+2dB
	0	0	0	0	0dB
	1	0	0	0	-2dB
	0	1	0	0	-4dB
	1	1	0	0	-6dB
	0	0	1	0	-8dB
	1	0	1	0	-10dB
	0	1	1	0	-12dB

Fader block

D45	D46	D47	D48	D49	D50	LFOUT
D51	D52	D53	D54	D55	D56	LROUT
D57	D58	D59	D60	D61	D62	RFOUT
D63	D64	D65	D66	D67	D68	RROUT
0	0	0	0	0	0	0dB

Pin Functions

Pin No.	Pin name	Function	Equivalent Circuit
36 35 34 42 43 44	L1 L2 L3 R1 R2 R3	Single end input pins.	
33 32 1 2	L4M L4P R4M R4P	Differential input pins.	
31 3	LSELO RSELO	Input selector output pins.	
30 4	LVRIN RVRIN	Main volume input pins.	
29 5	LCT RCT	Loudness function pins.	
24 10	LVROUT RVROUT	Tone output pins.	

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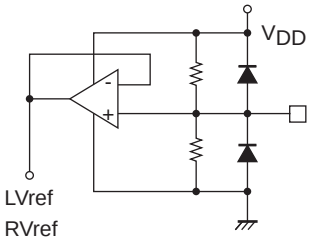
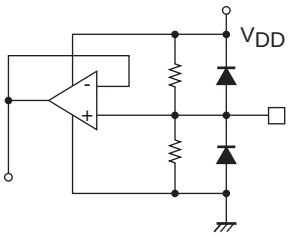
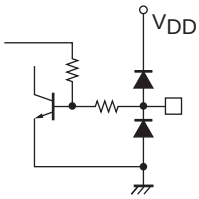
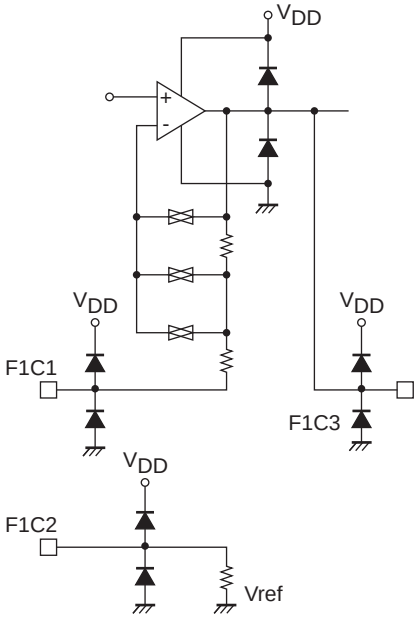
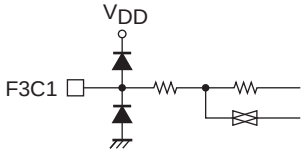
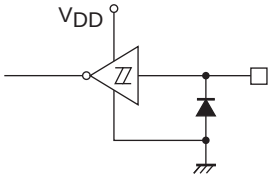
Pin No.	Pin name	Function	Equivalent Circuit
41	Vref	Connect a capacitor of a few tens of uF between Vref and AV_{SS} (V_{SS}) as a 0.55 V_{DD} voltage generator, current ripple countermeasure.	
15	VREG	Internal logic voltage pin.	
37	V_{DD}	Power supply pin.	
20	AV_{SS}	Ground pin.	
38	$\overline{MUTE}$	External muting control pin. Setting this pin to V_{SS} level sets forcibly fader volume block to - level.	
27 26 25 7 8 9	LF1C1 LF1C2 LF1C3 RF1C1 RF1C2 RF1C3	Capacitor connection pins for configuring equalizer bass band filter. Connect a capacitor between LF1C1 (RF1C1) and LF1C2 (RF1C2), and between LF1C2 (RF1C2) and LF1C3 (RF1C3).	
28 6	LF3C1 RF3C1	Capacitor connection pins for configuring equalizer treble band filter. Connect a high band compensation capacitor between LF3C1 (RF3C1) and V_{SS}.	
17 18	CL DI	Input pin for serial data and clock used for control.	
19	CE	Chip enable pin.Data is written to the internal latch and the analog switches are operated when the level changes from High to Low. Data transfer is enabled when the level is High.	

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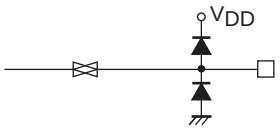
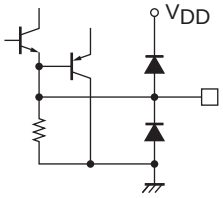
Pin No.	Pin name	Function	Equivalent Circuit
39	TEST	IC test pin. Normally this pin is OPEN.	
14	DV_{SS}	Logic system ground pin.	
16	OSC	External oscillat input pin. Normally this pin is OPEN.	
40	PH	Automatic zero cross detection pin.	

Usage Cautions

(1) Data Transmission at power on

The status of internal analog switches is unstable at power on. Therefore, perform muting or some other countermeasure until the data has been set.

At power on, initial setting data must be sent once in order to stabilize the bias of each block in a short time.

(2) Description of zero cross switching circuit operation