INTERNAL EQUIVALENT BLOCK DIAGRAM AND APPLICATION CIRCUIT

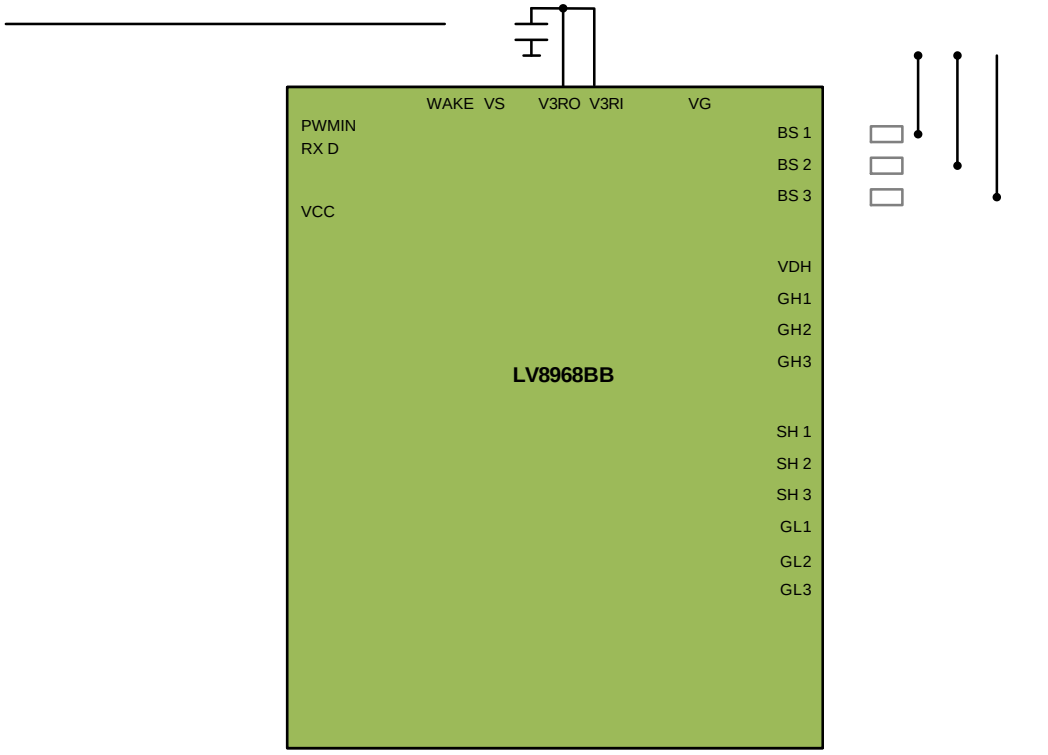


Figure 1. Typical Application Diagram

PIN ASSIGNMENT

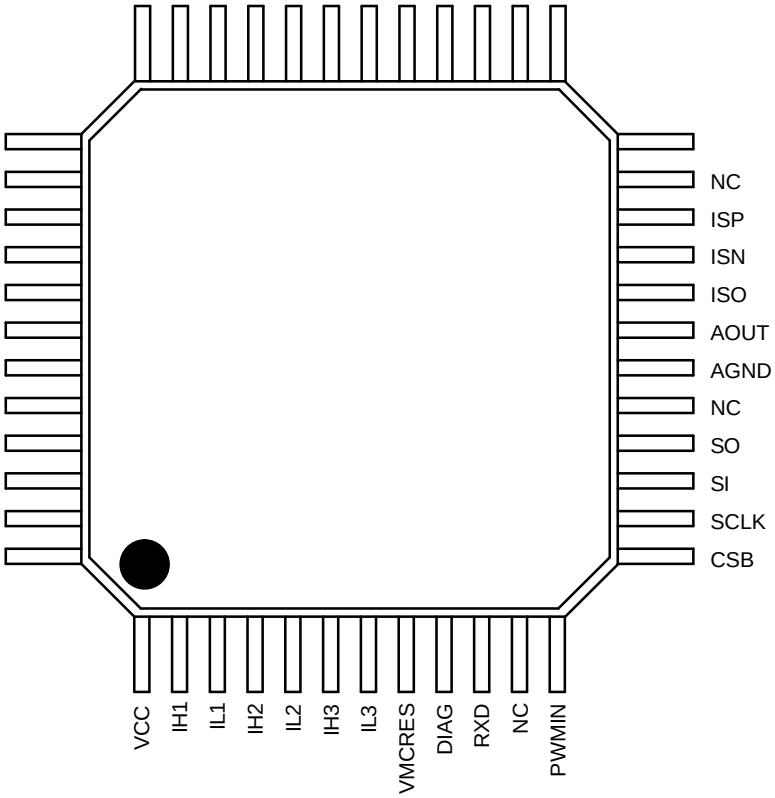


Figure 2. LV8968BB Pinout

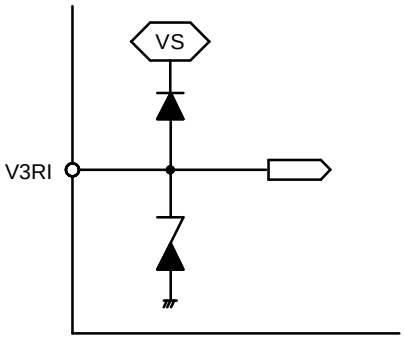
Table 1. PIN ASSIGNMENTS & DESCRIPTION (continued)

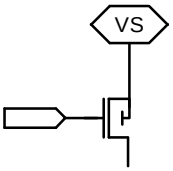
Name	No.	Description
SI	15	SPI interface serial data input pin.
SO	16	SPI interface serial data output pin. High level is pulled to VCC.
NC	17	No connection.
AGND	18	Ground pin.
AOUT	19	Output for various internal analog signals. Actual signal is selected via SPI register.
ISO	20	Output pin for current sense amplifier. Connect to AD converter input of the microcontroller for current sensing. Gain, reference, and overcurrent threshold is programmable via SPI register.
ISN	21	Current sense amp minus input pin. Connect this pin to the GND side of the shunt resistor with Kelvin leads.
ISP	22	Current sense amp plus input pin. Connect this through to top side of shunt resistor with Kelvin leads.
NC	23	No connection.
SL3	24	Low−side source connection of the power stage. Return path for gate current of GL3. Connect to source of FET controlled by IL3 or to common source of the power stage.
GL3	25	Gate driver output for low−side FETs. Switches voltage level between VG and SL3. Use at least 10 Ω gate resistors to protect against current spikes.
SH3	26	Connection for the motor phase terminal controlled by GH3 and GL3. Return path for high−side drivers and input for BEMF sensing.
GH3	27	Gate driver output for high−side FETs. Switches voltage level between BS3 and SH3. Use at least 10 Ω gate resistors to protect against current spikes.
BS3	28	Supply pin for high−side driver GH3. Needs a bootstrap capacitor to SH3 and a diode in reverse connection to VG.
SL2	29	Low−side source connection of the power stage. Return path for gate current of GL2. Connect to source of FET controlled by IL2 or to common source of the power stage.
GL2	30	Gate driver output for low−side FETs. Switches voltage level between VG and SL2. Use at least 10 Ω gate resistors to protect against current spikes.
SH2	31	Connection for the motor phase terminal controlled by GH2 and GL2. Return path for high−side drivers and input for BEMF sensing.
GH2	32	Gate driver output for high−side FETs. Switches voltage level between BS2 and SH2. Use at least 10 Ω gate resistors to protect against current spikes.
BS2	33	Supply pin for high−side driver GH2. Needs a bootstrap capacitor to SH2 and a diode in reverse connection to VG.
SL1	34	Low−side source connection of the power stage. Return path for gate current of GL1. Connect to source of FET controlled by IL1 or to common source of the power stage.
GL1	35	Gate driver output for low−side FETs. Switches voltage level between VG and SL1. Use at least 10 Ω gate resistors to protect against current spikes.
SH1	36	Connection for the motor phase terminal controlled by GH1 and GL1. Return path for high−side drivers and input for BEMF sensing.
GH1	37	Gate driver output for high−side FETs. Switches voltage level between BS1 and SH1. Use at least 10 Ω gate resistors to protect against current spikes.
BS1	38	Supply pin for high−side driver GH1. Needs a bootstrap capacitor to SH1 and a diode in reverse connection to VG.
VDH	39	Sense input for supply voltage and short−circuit detection of high−side power FETs. Connect through 100 Ω resistor to common drain of the power bridge.
VG	40	Power supply pin for low−side gate drive GL[1−3] directly and GH[1−3] through bootstrap circuit. Connect decoupling capacitor between VG and GND.
NC	41	No Connection.
VGIN	42	Gate supply input. Normally shorted to VS. Insert a charge pump circuit between VS and VGIN if low voltage operation is required.
VS	43	Power supply pin.

Table 1. PIN ASSIGNMENTS & DESCRIPTION (continued)

Name	No.	Description
WAKE	44	WAKE up pin for internal power supply. “H” => Operating mode, “L” or “Open” => Sleep mode.
NC	45	No connection.
EN	46	Active high digital input. A high on EN will activate the outputs. EN can be used as a hold input to allow an external microcontroller to keep the IC operating even if WAKE is low. A falling edge on EN clears the error flags.
V3RO	47	Internal regulator output pin. Connect capacitor between this pin and GND.
V3RI	48	Internal regulator feedback pin (Control circuit and Logic power supply). Connect to V3RO pin.

PIN FUNCTIONALITY





PIN FUNCTIONALITY (continued)

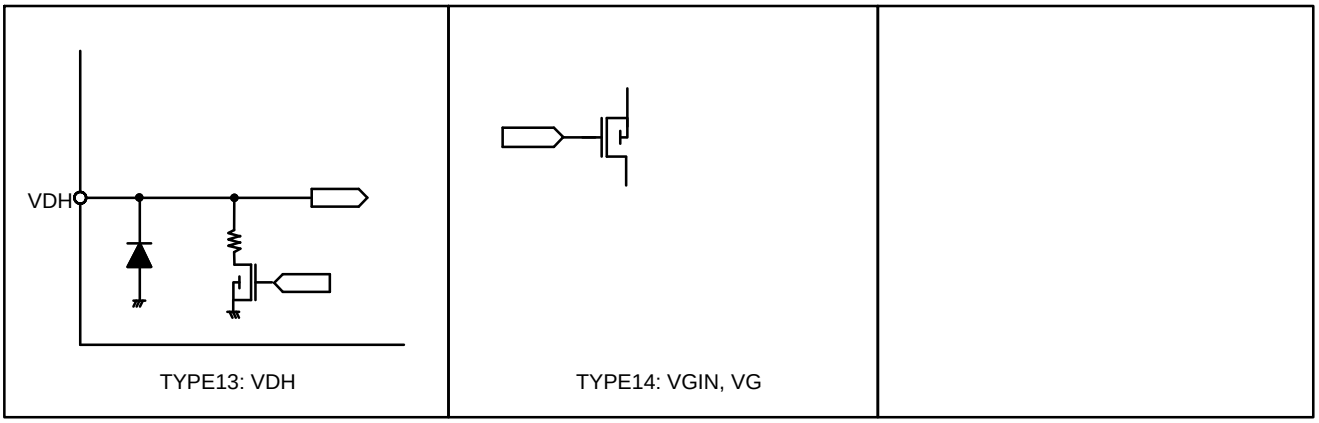


Figure 3. Pin Functionality

Table 3. ELECTRICAL CHARACTERISTICS
(Valid at a junction temperature range from −40°C to 150°C, for supply Voltage 8.0 V ≤ VS ≤ 25 V unless otherwise specified. Typical values at 25°C and VS = 12 V unless specified otherwise)

Table 3. ELECTRICAL CHARACTERISTICS (continued)
(Valid at a junction temperature range from −40°C to 150°C, for supply Voltage 8.0 V ≤ VS ≤ 25 V unless otherwise specified.
Typical values at 25°C and VS = 12 V unless specified otherwise)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
VG PIN						
VG output voltage	VGNO	Normal mode, VGVSEL = 0, IVG < 40 mA	7.0	11.0	12.0	V
	VGLO	Logic level mode, VGVSEL = 1	5	6	7	
	VGOL	VS = 6 V, IVG < 30 mA	5			
VG current limit	VGILIM					

Table 3. ELECTRICAL CHARACTERISTICS (continued)
(Valid at a junction temperature range from −40°C to 150°C, for supply Voltage 8.0 V ≤ VS ≤ 25 V unless otherwise specified.
Typical values at 25°C and VS = 12 V unless specified otherwise)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
DIGITAL OUTPUTS (SO)						
Output voltage	VSOH	Io = −1 mA	V_{VCC} −0.2			V
	VSOL	Io = 1 mA			0.2	V
OPEN DRAIN OUTPUTS (VMCRES, DIAG, RXD)						
Output voltage	VODL	Io = 1 mA			0.2	V
akage current	ILKOD	Vo = 5.5 V			10	μA
NING AND PROTECTION						
al warning ion temperature)	TWT0	THTSEL = 0	125			°C
	TWT1	THTSEL = 1	150			°C
	HYSTW	Hysteresis		25		°C
		THTSEL = 0	150			°C
ion temperature)	TSDT1	THTSEL = 1	175			°C

DETAILED FUNCTIONAL DESCRIPTION

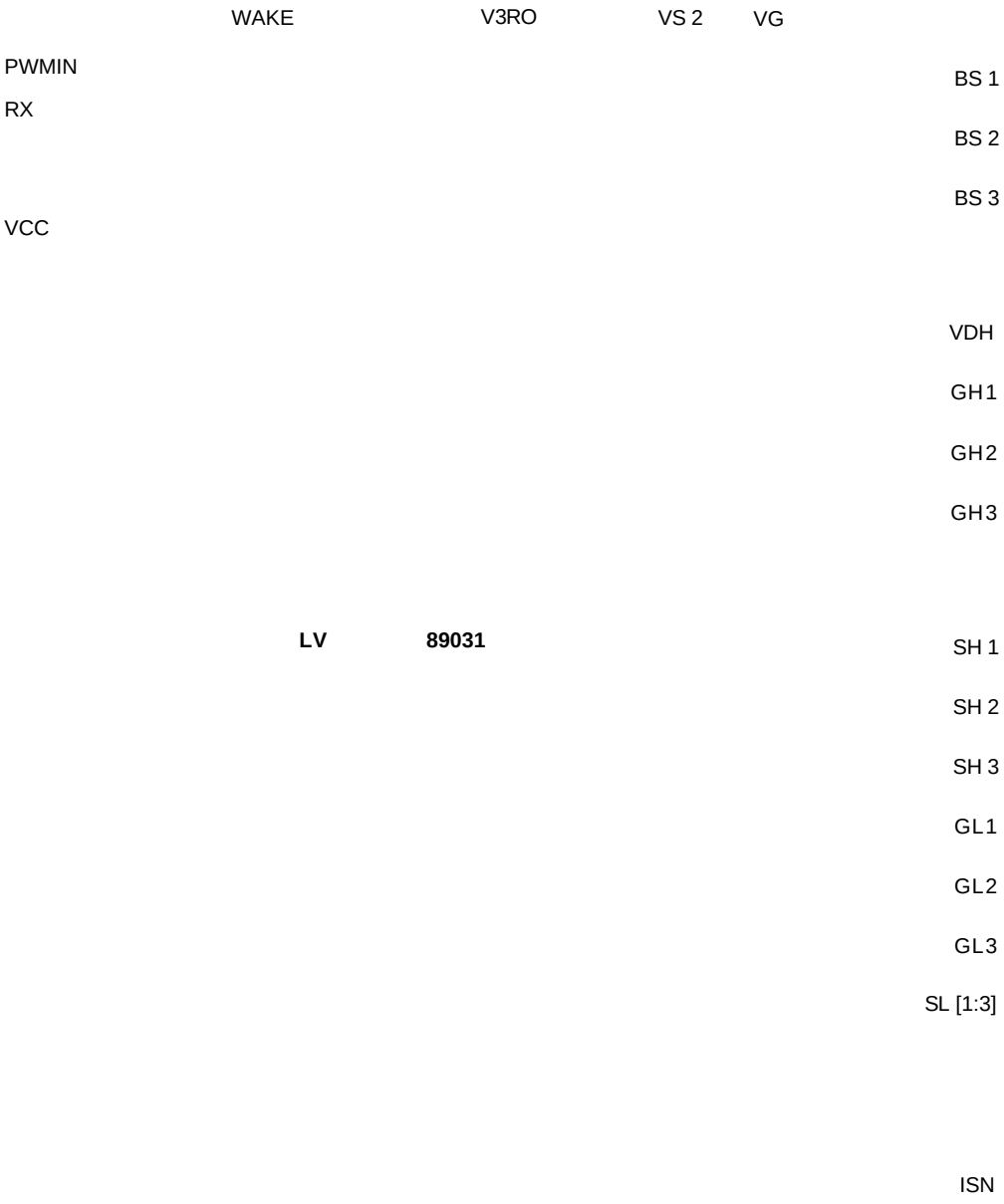


Figure 4. Block Diagram

Chip Activation, System States and Shutdown (EN, WAKE)

Once the supply voltage VS rises above VSLOF(Min.), the LV8968BB enters Sleep mode. In Sleep mode system states are controlled with pin WAKE.

Table 4. OPERATION MODES

Mode	WAKE	EN	V3RO	Logic	VCC	VG	SPI	Drivers
Sleep	L	NA	Disable	Reset	Disable	Disable	Disable	High−Z
Standby	H	L	Enable	Active	Enable	Enable	Enable	Low
Normal	NA	H	Enable	Active	Enable	Enable	Enable	Active

A high level on WAKE pin activates the IC from sleep mode and enables the internal linear regulator at V3RO. Once the voltage on V3RO as sensed on V3RI has passed the power on reset (POR) threshold the system oscillator starts, and releases the internal digital reset. OTP register contents are loaded into the system registers defining the power on state of the LV8968BB and the VCC regulator voltage.

VCC is powering up next, holding the CPU reset line VMCRES low until VCC passes its undervoltage level. During the entire wake−up sequence, DIAG is masked for VG undervoltage. After wake−up is complete, the IC enters Standby mode and DIAG is activated to display internal errors. During Standby mode full SPI access is possible.

Note that if the CPU watchdog was enabled via OTP, a VMCRES low will be asserted after the watchdog first open window (WDFOW) unless the watchdog is being triggered properly. See section “

Operating Voltage Range

Normal operation with full functionality is guaranteed from 8 V to 25 V. The device will operate from 4.5 V to 40 V with limited performance:

Shutdown: VS < $VSLOF_{(min)}$

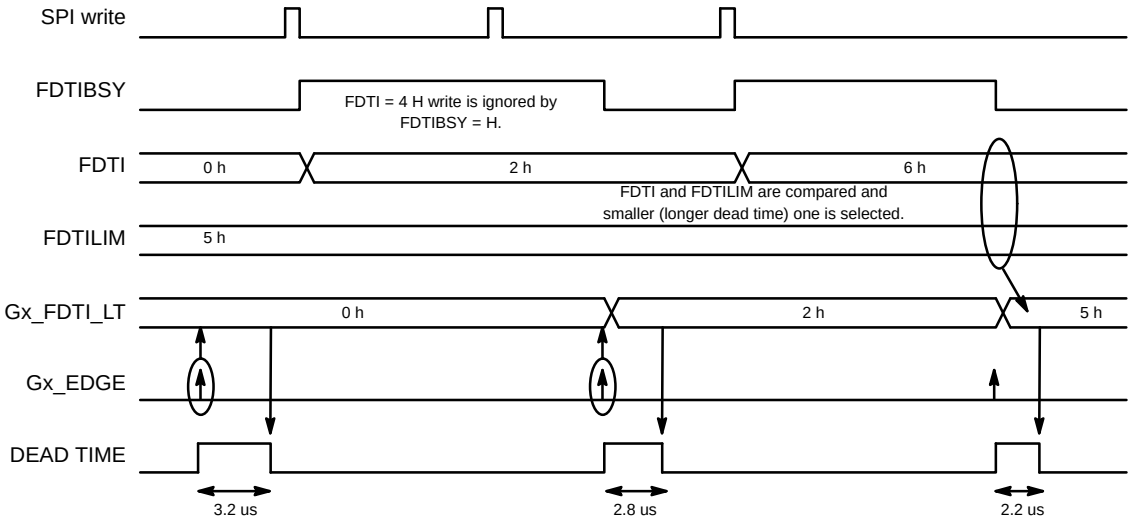


Figure 6. Dead Time Programming

Short Protection

To protect against FET shorts the drain−source voltage of the active external power FETs is monitored. The drain source voltage of the high−side FETs is monitored between VDH and the corresponding source SH[1−3]. While the low−side FETs are monitored between SH[1−3] and SL[1−3]. After activation of the FET the short detection is masked for time t_{FSFT} to allow for signal settling. If after the masking time t_{FSFT} the FET voltage exceeding V_{FSDL} continues for t_{FSDT}, a FET short error is flagged. For details see “System Errors and Warnings” on page 18.

Four bits register FSDL selects the FET short protection shutoff voltage VFSDL. The masking time TFSDT is set with bits FSDT[1:0] and a debounce filter time TFSFT is set with bits FSFT[1:0]. Both parameters residing in register MRCONF6. These registers are dynamic and FSDL can be changed during motor operation, though FSFT and FSDT can be changed when EN = L.

Current Sensing and Overcurrent Shutoff

Single shunt current sensing can be implemented with the integrated high speed sense amplifier. It amplifies the voltage across ISP – ISN with a programmable gain defined by register CSGAIN. Access to this register is dynamic, allowing gain adjustment during motor operation. The offset is determined by CSOFEN relative to an internal reference which can be either 200 mV(typ) for unidirectional current sensing, or 1.5 V(typ) for sensing current in both directions. The output of the current sense amplifier appears on the ISO pin.

Overcurrent Shutoff

A parallel path implements fast overcurrent shutoff of the driver stage. Overcurrent shutoff is triggered if the voltage across ISP − ISN exceeds a programmable level as defined by register OCDL. In overcurrent shutoff all gate drivers go to Hi−Z, turning the power FETs high impedance and letting the motor freewheel – this reaction is maskable. For more information on masking and recovery see section “System Errors and Warnings” on page 18.

To suppress switching transients, an overcurrent masking time can be programmed into register OCMASK.

Temperature Sensing

The LV8968BB monitors internal junction temperature T_j. The voltage representing this temperature (V_{PTAT}) can be sampled at AOUT as described below. Thermal warnings and errors are issued if T_J exceeds the levels defined by THTSEL:

Table 7. THERMAL THRESHOLDS

THTSEL	Thermal Warning	Thermal Shutoff
0	125°C	150°C
1	150°C	175°C

If thermal error shutoff is activated, VG85 0 .[(activated, S 1)17(ucb 1W*n0 792 61 ernal jun8m.1143706 Tw[(the active exte1 Twed if T)]15.

Table 9. WINDOW WATCHDOG TIMING OPTIONS (T_J = −40 to 150 °C, VS = 4.5 to 40 V)

Symbol	Characteristic	Min	Typ	Max	Unit
T_{FOW}	WDT first open window time				ms
	WDTWT[2:0] = 0h	390.0	409.6	431.2	
	WDTWT[2:0] = 1h	195.0	204.8	215.6	
	: (1/2 step)	:	: (1/2 step)	:	
	WDTWT[2:0] = 7h	3.0	3.2	3.4	
T_{CW}	WDT closed window time				ms
	WDTWT[2:0] = 0h	97.4	102.4	107.8	
	WDTWT[2:0] = 1h	48.7	51.2	53.9	
	: (1/2 step)	:	:(1/2 step)	:	
	WDTWT[2:0] = 7h	0.7	0.8	0.9	
T_{WT}	WDT window time				ms
	WDTWT[2:0] = 0h	195.0	204.8	215.6	
	WDTWT[2:0] = 1h	97.4	102.4	107.8	
	: (1/2 step)	:	:(1/2 step)	:	
	WDTWT[2:0] = 7h	1.4	1.6	1.7	
T_{MR}	WDT microcontroller reset time	333	400	422	μs

System Errors and Warnings

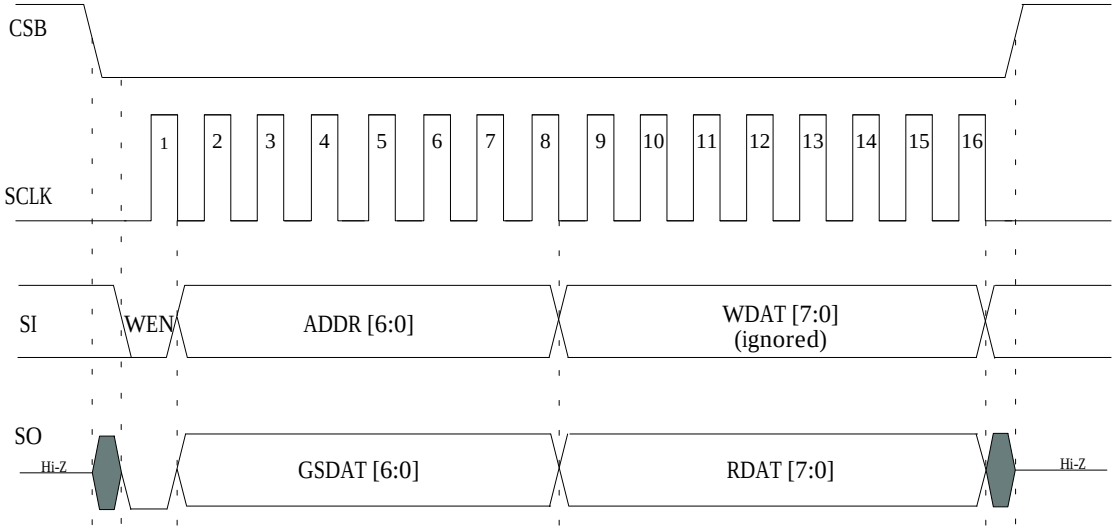


Figure 9. SPI Format in Read Mode

SPI communications with the LV8968BB follows established industry standard practices

The following SPI failures are detectable and reported collectively by a high on SACF in GSDAT[5] as general SPI failures:

- Any access to an address which is not assigned.
- The number of SCLK edges is not 16 within one word transfer
- Any access to MRCONF and ORCONF while OBSY = 1, (During write operations)
- Write access to MRODL register while OBSY = 1, (during write operations)
- Write access to any of the main registers after setting MSAENB = 1 (Implies Reg. address 04 h to 075h are locked)
- Write access to any of the OTP registers after OSAENB = 1 (Implies Reg. address 40 h to 435h are locked)
- Write access attempt to a read only or locked register
- SI signal changed at positive edge of SCLK (Incorrect data/sclk phase setup)
- Write access to dead time register FDTI while FDTIBSY is still high (last value has not been uploaded)

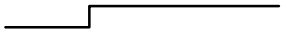


Figure 12. OTP Data Download Timing after an MRODL Command

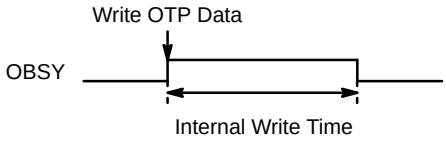


Figure 14. OTP Programming Timing

The programming takes 4 ms maximum. To simplify operation, a waiting for 4 ms plus margin can be applicable instead of a polling of the flag OBSY. (Figure 15)

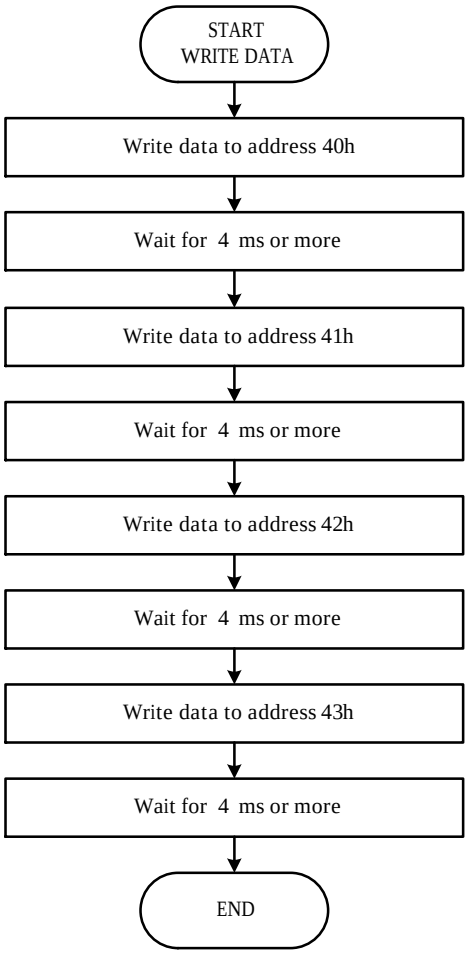


Figure 15. OTP Memory Write and Verify Flow

OTP Data Integrity Verification

In order to verify that the OTP programming operation was successful. It is strongly recommended to do an OTP margin check: To do this, the OTP registers are downloaded into the main register bank with minimum and maximum readout thresholds. This OTP download is forced by writing 00h to register MRODL. The readout threshold is set in register MRORB.

OTP Margin read check sequence after programmed:

1. Set OTP readout threshold “low” by setting ORBEN = 1 and ORBLV = 0 in register MRORB
2. Execute OTP download command by writing 00h to MRODL
3. Verify that the main register contents are consistent with the programmed OTP data
4. Set OTP readout threshold “high” by setting ORBEN = 1 and ORBLV = 1 in register MRORB
5. Execute OTP download command by writing 00h to MRODL
6. Verify that the main register contents are consistent with the programmed OTP data
7. Return OTP threshold to normal by setting ORBEN = 0 and ORBLV = 0
8. Execute OTP download command
9. Verify that the main register contents are consistent with the programmed OTP data

Locking OTP Register Contents

MSAENB bit and OSAENB bit are used in order to prevent write−access of main− and OTP registers respectively.

CAUTION: Inadvertent writing of these bits will permanently lock the corresponding register blocks from any further write access. Should only be set at end of development cycles.

Table 13. REGISTER MAP

WENB by WEN (1bit)	Write Time Condition	ADDR [6:0]	Data Name	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Don't care	Don't care	–	GSDAT	0	ORBEN	SACF	DIAGS	LATCH	OBSY	SMOD[1:0]	
OSAENB (Note 10)	EN=L	00h	MRCONF0	0	0	THTSEL	DFCSEL	DIAGLTO	DIAGPOL	VGVSEL	VCVSEL
		01h	MRCONF1	0	0	0	WDTPS	THSPS	THWPS	VGUVPS[1:0]	
		02h	MRCONF2	0	0	VDOVPS[1:0]		VSOVPS[1:0]		VSUVPS[1:0]	
Read Only	Read Only	03h	MRCONF3	0	0	0	0	0	0	0	OSAENB
MSAENB (Note 10)	EN=L	04h	MRCONF4	0	WDTWT[2:0]			0	CSOFEN	AWODLEN	D3MDEN
		05h	MRCONF5	0	0	OCDL[1:0]		OCMASK[3:0]			
		06h	MRCONF6	0	0	0	0	FSFT[1:0]		FSDT[1:0]	
		07h	MRCONF7	FSPS[1:0]		OCPS[1:0]		FDTILIM[3:0]			
EN=L or H		08h	MRCONF8	0	0	0	0	0	0	0	MSAENB
EN=L or H	EN=L or H	10h	MRAOSEL	0	0	0	0	0	AOUTSEL[2:0] (Default=7h)		
		11h	MRCSG	0	0	0	0	0	0	CSGAIN[1:0]	
		12h	MRFSDL	0	0	0	0	FSDL[3:0]			
		13h	MRFDTI	0	0	0	0	FDTI[3:0]			
		14h	MRFDTIF	0	0	0	0	0	0	0	FDTIBSY
		15h	MRRST	Write 00h: Reset WDT / Write FFh: Reset latch off							
	EN=L	16h	MRORB	0	0	0	0	0	0	ORBEN	ORBLV
		17h	MRODL	Write 00h: Execute OTP data download							
Read Only	Read Only	20h	MRDIAG0	0FDTIB2376.441 432436 283.1811 422.7024 Tm76.441 432436 283.18115.241 371 refBT6 0 0 6 192.7559 382.3937 T5885.3354 382.393							

MRCONF0 (Default: 00h)
(Write Access Only when EN = Low. OTP Backup Possible)

ADDR	Data Name	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
00h	MRCONF0	0	0	THTSEL	DFCSEL	DIAGLTO	DIAGPOL	VGVSEL	VCVSEL

THTSEL: THermal Thresholds SELection
Temperature warning threshold and error selection.
- THTSEL = 0: Thermal warning = 125°C, Thermal shutdown = 150°C
- THTSEL = 1: Thermal warning = 150°C, Thermal shutdown = 175°C

DFCSEL: Diag Flag Clearing SELection
Defines the condition under which the error registers are reset, by error condition removed only, or by error condition removed and subsequent SPI read access of the register in question.
- DFCSEL = 0: If error was cleared, DIAGS flag of GSDAT and MRDIAG0 and MRDIAG1 flags are reset by MRDIAG0 read, MRDIAG1 read
- DFCSEL = 1: DIAGS flag of GSDAT and MRDIAG0 and MRDIAG1 flag are reset by recovery condition

DIAGLTO: DIAG pin Latched errors Transition Only
If this bit is set, only latched errors result in a transition on DIAG. Otherwise all errors (and warnings) will be flagged.
- DIAGLTO = 0: At the time of detecting auto recover or latch off error, DIAG output is on
- DIAGLTO = 1: At the time of detecting latch off error, DIAG output is on

DIAGPOL: DIAG pin POLarity
Decides the polarity of the DIAG output.
- DIAGPOL = 0: At the time of detecting diagnostic error, DIAG output is L
- DIAGPOL = 1: At the time of detecting diagnostic error, DIAG output is H

VGVSEL: VG pin Voltage SELection
Selects if the IC is in logic level mode or normal mode which modifies the gate voltage of the drive section.
- VGVSEL = 0: VG normal mode (VG = 11 V)
- VGVSEL = 1: VG logic level mode (VG = 6 V)

VCVSEL: VCc pin Voltage SELection
Selects the output voltage of VCC to be either 3.3 V or 5 V. The wrong bit selection has a possibility to damage the microcontroller. Please make sure the appropriate selection.
- VCVSEL = 0: VCC = 3.3 V
- VCVSEL = 1: VCC = 5.0 V

MRCONF1 (Default: 00h)
(Write Access Only when EN = Low. OTP Backup Possible)

ADDR	Data Name	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
01h	MRCONF1	0	0	0	WDTPS	THSPS	THWPS	VGUVPS[1:0]	

WDTPS: WatchDog Timeout Protection Setting
Watchdog error results in error response or is ignored.
- WDTPS = 0: Ignore WDT error
- WDTPS = 1: Emergency off and report a WDT error (Auto recover)

THSPS: THermal Shutdown Protection Setting
Thermal shutdown error results in error response or is ignored.
- THSPS = 0: Ignore thermal shutdown error
- THSPS = 1: Emergency off and report at thermal shutdown error (Auto recover)

THWPS: THermal Warning Protection Setting
- THWPS = 0: Ignore thermal warning error
- THWPS = 1: Report thermal warning error

VGUVPS[1:0]: VG pin UnderVoltage Protection Setting

- VGUVPS[1:0] = 0h: Ignore VG undervoltage error
- VGUVPS[1:0] = 1h: Report VG undervoltage error ♦
- VGUVPS[1:0] = 2h, 3h: Emergency off and report at VG under voltage error (Auto recover)

MRCONF2 (Default: 00h)

(Write Access Only when EN = Low. OTP Backup Possible)

ADDR	Data Name	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
02h	MRCONF2	0	0	VDOVPS[1:0]		VSOVPS[1:0]		VSUVPS[1:0]	

VDOVPS[1:0]: VDh OverVoltage Protection Setting

- VDOVPS[1:0] = 0h: Ignore VDH overvoltage error
- VDOVPS[1:0] = 1h: Report VDH overvoltage error
- VDOVPS[1:0] = 2h, 3h: Emergency off and report at VDH over voltage error (Auto recover)

VSOVPS[1:0]: VS OverVoltage Protection Setting

- VSOVPS[1:0] = 0h: Ignore VS overvoltage error
- VSOVPS[1:0] = 1h: Report VS overvoltage error
- VSOVPS[1:0] = 2h, 3h: Emergency off and report at VS over voltage error (Auto recover)

VSUVPS[1:0]: VS UnderV♦

MRCONF4 (Default: 00h)
(Write Access Only when EN = Low)

ADDR	Data Name	D[7]	D[6]

MRCONF6 (Default: 00h)
(Write Access Only when EN = Low)

ADDR	Data Name	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
06h	MRCONF6	0	0	0	0	FSFT[1:0]		FSDT[1:0]	

FSFT[1:0]: Fet Short detection debounce Filter Time
External FET short detection debounce time. A short condition has to remain valid during this time.
- FSFT[1:0] = 0h: FET short detect time = 0.8 μs
- FSFT[1:0] = 1h: FET short detect time = 1.6 μs
- FSFT[1:0] = 2h: FET short detect time = 2.4 μs
- FSFT[1:0] = 3h: FET short detect time = 3.2 μs

FSDT[1:0]: Fet Short Detection masking Time
External FET short−circuit detection masking time, starts after turn−on of the FET.
- FSDT[1:0] = 0h: FET short masking time = 3.2 μs
- FSDT[1:0] = 1h: FET short masking time = 6.4 μs
- FSDT[1:0] = 2h: FET short masking time = 9.6 μs
- FSDT[1:0] = 3h: FET short masking time = 12.8 μs

MRCONF7 (Default: 00h)
(Write Access Only when EN = Low)

ADDR	Data Name	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
07h	MRCONF7	FSPS[1:0]		OCPS[1:0]		FDTILIM[3:0]			

FSPS[1:0]: Fet Short−circuit error Protection Setting
Short−circuit error decision mask.
- FSPS[1:0] = 0h: Ignore FET short error
- FSPS[1:0] = 1h: Report FET short error
- FSPS[1:0] = 2h: Emergency off and report at FET short error (Auto recover)
- FSPS[1:0] = 3h: Emergency off and report at FET short error (Latched off)

OCPS[1:0]: OverCurrent error Protection Setting
Overcurrent error decision mask.
- OCPS[1:0] = 0h: Ignore overcurrent error
- OCPS[1:0] = 1h: Report overcurrent error
- OCPS[1:0] = 2h: Emergency off and report at overcurrent error (Auto recover)
- OCPS[1:0] = 3h: Emergency off and report at overcurrent error (Latched off)

FDTILIM[3:0]: Fet Dead TIme LIMit
Minimum Dead time programming register.
- FDTILIM[3:0] = 0h: FET dead time = 3.2 μs
- FDTILIM[3:0] = 1h: FET dead time = 3.0 μs
  :
  : (−0.2 μs step)
  :
- FDTILIM[3:0] = Eh: FET dead time = 0.4 μs
- FDTILIM[3:0] = Fh: FET dead time = 0.2 μs

MRCONF8 (Default: 00h)
(Write access only when EN = Low)

ADDR	Data Name	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
08h	MRCONF8	0	0	0	0	0	0	0	MSAENB

MSAENB: Mrconf Spi write Access ENable Bar
Setting this bit disables all write access to the configuration registers MRCONF4 to MRCONF7.
- MSAENB = 0: Enable write access of MRCONF4 ~ 7
- MSAENB = 1: Disable write access of MRCONF4 ~ 7

MRAOSEL (Default: 07h)
(Full Dynamic Access)

ADDR	Data Name	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
10h	MRAOSEL	0	0	0	0	0	AOUTSEL[2:0]		

AOUTSEL[2:0]: AOUT pin output SELect
Select the internal nodes brought out on AOUT.
- AOUTSEL[2:0] = 0h: AOUT = Output VDH voltage level
- AOUTSEL[2:0] = 1h: AOUT = Output SH1 voltage level
- AOUTSEL[2:0] = 2h: AOUT = Output SH2 voltage level
- AOUTSEL[2:0] = 3h: AOUT = Output SH3 voltage level
- AOUTSEL[2:0] = 4h, 5h: AOUT = Output thermal monitor voltage level
- AOUTSEL[2:0] = 6h, 7h: AOUT = Hi−Z

MRCSG (Default: 00h)
(Full Dynamic Access)

ADDR	Data Name	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
11h	MRCSG	0	0	0	0	0	0	CSGAIN[1:0]	

CSGAIN[1:0]: Current Sense GAIN
Programs the gain of the current sense amplifier.
- CSGAIN[1:0] = 0h: Current sense amp gain = 7.5
- CSGAIN[1:0] = 1h: Current sense amp gain = 15
- CSGAIN[1:0] = 2h: Current sense amp gain = 22.5
- CSGAIN[1:0] = 3h: Current sense amp gain = 30

MRFSDL (Default: 00h)
(Full Dynamic Access)

ADDR	Data Name	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
12h	MRFSDL	0	0	0	0	FSDL[3:0]			

FSDL[3:0]: Fet Short Detection Level
Defines the maximum allowable drain source voltage across a power FET.
- FSDL[3:0] = 0h: FET short detect level = 100 mV
- FSDL[3:0] = 1h: FET short detect level = 200 mV
  :
  : (100 mV step)
  :
- FSDL[3:0] = Eh: FET short detect level = 1500 mV
- FSDL[3:0] = Fh: FET short detect level = 1600 mV

MRFDTI (Default: 00h)
(Full Dynamic Access)

ADDR	Data Name	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
13h	MRFDTI	0	0	0	0	FDTI[3:0]			

FDTI[3:0]: Fet Dead TIme

Dead time programming register. This dead time will be applied unless it is smaller than FDTILIM[3:0] in MRCONF7.

- FDTI[3:0] = 0h: FET dead time = 3.2 μs
- FDTI[3:0] = 1h: FET dead time = 3.0 μs

  :

  : (−0.2 μs step)

  :
- FDTI[3:0] = Eh: FET dead time = 0.4 μs
- FDTI[3:0] = Fh: FET dead time = 0.2 μs

MRFDTIF (Default: 00h)
(Full Dynamic Access)

ADDR	Data Name	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
14h	MRFDTIF	0	0	0	0	0	0	0	FDTIBSY

FDTIBSY: Fet Dead TIme BuSY uploading

FDTIBSY goes high after the dead time register was written to via SPI but not uploaded into the dead time counter. Upload happens at the beginning of every dead time measuring period (falling edge of a gate signal) and clears the FDTIBSY flag.

A write access MRFDTIF = 01h also clears the FDTIBSY flag.

MRRST
(Full Dynamic Access)

ADDR	Data Name	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
15h	MRRST	Write 00h: Reset WDT / Write FFh: Reset latch off							

MRRST[7:0]: Master Register ReSeT

Write access to this register resets the Watchdog or the Error latch.

- Write MRRST[7:0] = 00h: Reset WDT
- Write MRRST[7:0] = FFh: Reset latch off

MRORB (Default: 00h)
(Register for OTP Programming Integrity Check. Write During EN = Low Only)

ADDR	Data Name	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
16h	MRORB								

MRODL
(Write Access During EN = Low Only)

ADDR	Data Name	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
17h	MRODL	Write 00h: Execute OTP data download							

MRODL[7:0]: Master Register Otp DownLoad

A write initiates an OTP data download into the main registers in standby mode. In Normal mode, OTP download can be initiated only when AWODLEN is set regardless of MRODL.

- Write MRODL[7:0] = 00h: Execute OTP data download

MRDIAG0
(Read Only)

ADDR	Data Name	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
20h	MRDIAG0	0	0	0	WDTPO	THSPO	THWPO	FSPO	OCPO

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CASE 131AN
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