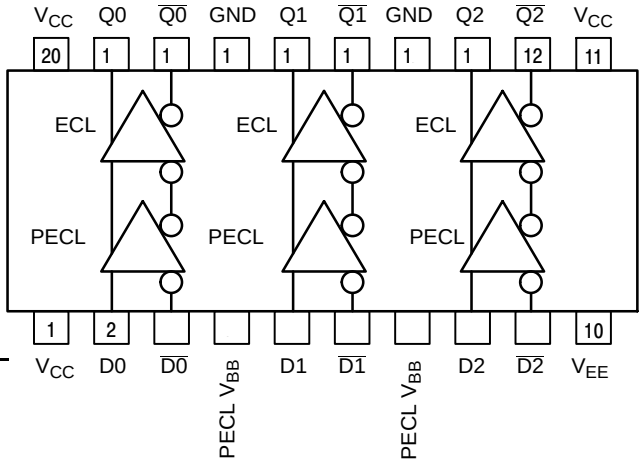

**All V_{CC} pins are tied together on the die.

Warning: All V_{CC}, V_{EE}, and GND pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. 20-Lead Pinout (Top View) **and Logic Diagram**

Table 1. PIN DESCRIPTION

PIN	FUNCTION
Dn, $\overline{Dn}$	PECL Inputs
Qn, $\overline{Qn}$	ECL Outputs
PECL V_{BB}	PECL Reference Voltage Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply
GND	Ground

Table 2. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	PECL Power Supply	GND = 0 V		8 to 0	V
V_{EE}	NECL Power Supply	GND = 0 V		−8 to 0	V
V_I	PECL Input Voltage	GND = 0 V	V_I V_{CC}	6 to 0	V
I_{out}	Output Current	Continuous Surge		50 100	mA
I_{BB}	PECL V_{BB} Sink/Source			0.5	mA
T_A	Operating Temperature Range			−40 to +85	

Table 3. PECL INPUT DC CHARACTERISTICS (V_{CC}= 5.0 V; V_{EE}= −5.0 V; GND = 0 V.) (Note 1)

Symbol	Characteristic	−40 C			25 C			85 C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{CC}	V_{CC} Power Supply Current			11		6	11			11	mA
V_{IH}	Input HIGH Voltage (Single-Ended)	3835		4120	3835		4120	3835		4120	mV
V_{IL}	Input LOW Voltage (Single-Ended)	3190		3525	3190		3525	3190		3525	mV
PECL V_{BB}	Output Voltage Reference	3.62		3.74	3.62		3.74	3.62		3.74	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 2) V_{PP} < 500 mV V_{PP} 500 mV	 1.3 1.5		 4.8 4.8	 1.2 1.4		 4.8 4.8	 1.2 1.4		 4.8 4.8	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

1. Input parameters vary 1:1 with V_{CC}. V_{CC} = +4.75 V to +5.2 V, V_{EE} = −4.20 V to −5.5 V.
2. V_{IHCMR} min varies 1:1 with GND. V_{IHCMR} max varies 1:1 with V_{CC}.

Table 4. NECL OUTPUT DC CHARACTERISTICS (V_{CC}= 5.0 V to 5.0 V; V_{EE}= −5.0 V; GND= 0 V.) (Note 1)

Symbol	Characteristic	−40 C			25 C	85 C	Unit
		Min	Typ	Max	Min		

Table 5. AC CHARACTERISTICS (V_{CC}= 5.0 V; V_{EE}= −5.0 V; GND= 0 V.) (Note 4)

Symbol	Characteristic	−40 C			25 C			85 C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency		700			700			700		MHz
t_{PLH} t_{PHL}	Propagation Delay D to Q Differential Single-Ended.	 540 490	 640 640	 740 790	 570 520	 670 670	 770 820	 610 560	 710 710	 810 860	ps
t_{SKEW}	Skew Output-to-Output (Note 1) Part-to-Part (Differential) (Note 1) Cycle (Differential) (Note 2)		 40 25	 100 200		 40 25	 100 200		 40 25	 100 200	ps
t_{JITTER}	Random Clock Jitter @ 700 MHz		1.2			1.2			1.2		pS(RMS)
V_{PP}	Input Swing (Note 3)	200		1000	200		1000	200		1000	mV
t_r t_f	Output Rise/Fall Times Q (20% − 80%)	270	400	530	270	400	530	270	400	530	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

1. Skews are valid across specified voltage range, part-to-part skew is for a given temperature.
2. Duty cycle skew is the difference between a t_{PLH} and t_{PHL} propagation delay through a device.
3. V_{PP}(min) is the minimum input swing for which AC parameters are guaranteed. The device has a DC gain of 40.
4. V_{CC} = +4.75 V to +5.2 V, V_{EE} = −4.20 V to −5.5 V. Outputs are terminated through a 50 Ω resistor to GND − 2.0 V.

Figure 2. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D

Resource Reference of Application Notes

AN1405/D − ECL Clock Distribution Techniques

AN1406/D − Designing with PECL (ECL at +5.0 V)

AN1503/D − ECLinPS™ I/O SPiCE Modeling Kit

AN1504/D − Metastability and the ECLinPS Family

AN1568/D − Interfacing Between LVDS and ECL

AN1672/D − The ECL Translator Guide

AND8001/D − Odd Number Counters Design

AND8002/D − Marking and Date Codes

AND8020/D − Termination of ECL Logic Devices

AND8066/D − Interfacing with ECLinPS

AND8090/D − AC Characteristics of ECL Devices

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