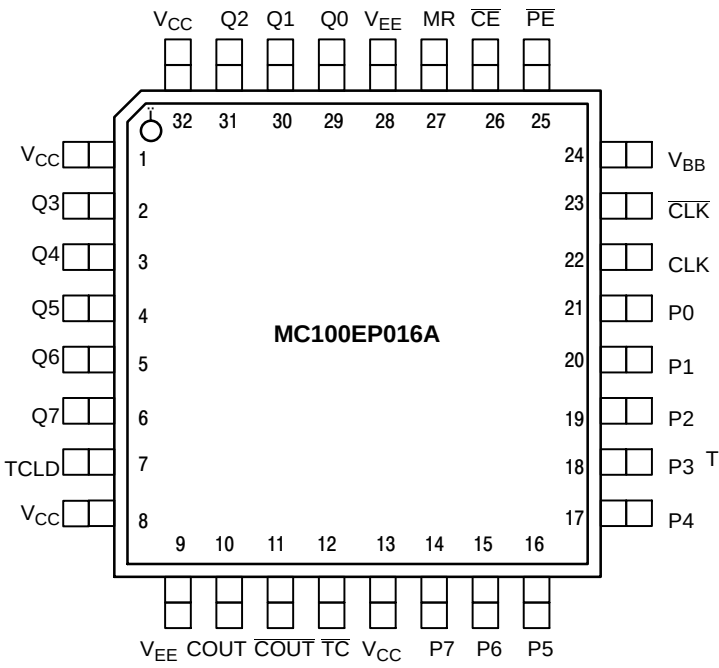
3.3 V ECL 8-Bit Synchronous Binary Up Counter

MC100EP016A

Description

The MC100EP016A is a high−speed synchronous, presettable, cascadeable 8−bit binary counter. Architecture and operation are the same as the ECLinPS family MC100E016 with higher operating speed.

The counter features internal feedback to $\overline{TC}$ gated by the TCLD (Terminal Count Load) pin. When TCLD is LOW (or left open, in which case it is pulled LOW by the internal pulldowns), the $\overline{TC}$ feedback is disabled, and counting proceeds continuously, with $\overline{TC}$ going LOW to indicate an all−one state. When TCLD is HIGH, the TC feedback causes the counter to automatically reload upon TC = LOW, thus functioning as a programmable counter. The Qn outputs do not need to be terminated for the count function to operate properly. To minimize noise and power, unused Q outputs 6.2res integ mA5T10 0 017.3(Q)1TT5 1 Tf13.020. -.0021 Tc(For additi



Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. 32−Lead LQFP Pinout (Top View)

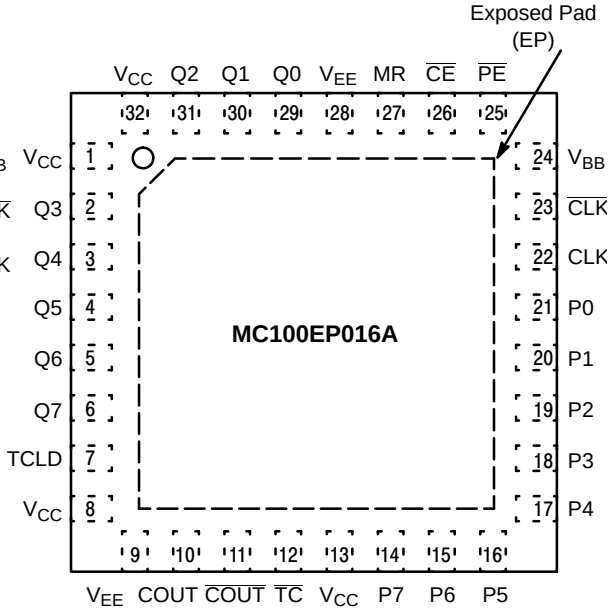


Figure 2. 32−Lead QFN Pinout (Top View)

Table 1. PIN DESCRIPTION

Pin

CL(Data OutputsC)Tj ET 179032 7-39417 .9019 15.307 N DES532.189 7-39417 .9019 15.307 N DE 179032 388347537-3.76t3.36645 re f BT 8 0 0 8694. 36]3.9109 Tm 0 To

Table 4. ATTRIBUTES

Characteristics	
Internal Input Pulldown Resistor	
Internal Input Pullup Resistor	
ESD Protection	Human Body Model Machine Model Charged Device Model
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)	
	LQFP−32 QFN−32
Flammability Rating Oxygen Index: 28 to 34	
Transistor Count	
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note AND8003/D.

Table 5. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V	
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V	
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	V_I V_I
I_{out}	Output Current	Continuous Surge	
I_{BB}	V_{BB} Sink/Source		
T_A	Operating Temperature Range		
T_{stg}	Storage Temperature Range		
θ_{JA}	Thermal Resistance (Junction−to−Ambient) QFN	0 lfpm500 lfpm32 500 lfpm	32 32

Table 6. 100EP DC CHARACTERISTICS, PECL V_{CC} = 3.3 V, V_{EE} = 0 V (Note 2)

		−40°C	25°C	70°C	
Symbol	**Characteristic**				**UnitCharacteristic**

Table 8. AC CHARACTERISTICS V_{EE} = −3.0 V to −3.6 V; V_{CC} = 0 V or V_{CC} = 3.0 V to 3.6 V, V_{EE} = 0 V (Note 8)

		−40°C			25°C			70°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{COUNT}	Maximum Frequency Count & Division Modes Q, $\overline{TC}$, COUT/$\overline{COUT}$	1.3	1.5		1.2	1.4					

APPLICATIONS INFORMATION

Cascading Multiple EP016A Devices

For applications which call for larger than 8-bit counters

APPLICATIONS INFORMATION (continued)

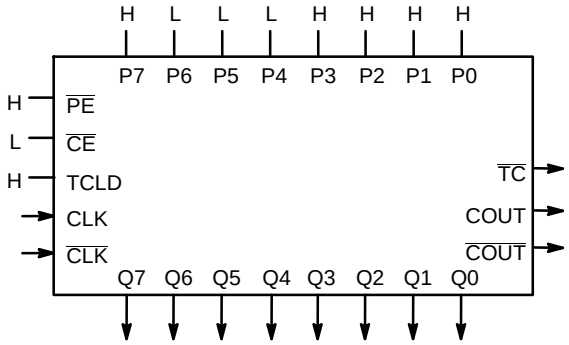


Figure 5. Mod 2 to 256 Programmable Divider

To determine what value to load into the device to accomplish the desired division, the designer simply subtracts the binary equivalent of the desired divide ratio from the binary value for 256. As an example for a divide ratio of 113:

Pn's = 256 − 113 = $8F_{16}$ = 1000 1111

where:

P0 = LSB and P7 = MSB

Forcing this input condition as per the setup in Figure 5 will result in the waveforms of Figure 6. Note that the $\overline{TC}$ output is used as the divide output and the pulse duration is equal to a full clock period. For even divide ratios, twice the desired divide ratio can be loaded into the EP016A and the $\overline{TC}$ output can feed the clock input of a toggle flip flop to aivius 1 0 0 RCLK0 0 2 TD2divTD-338 7.80R

APPLICATIONS INFORMATION (continued)

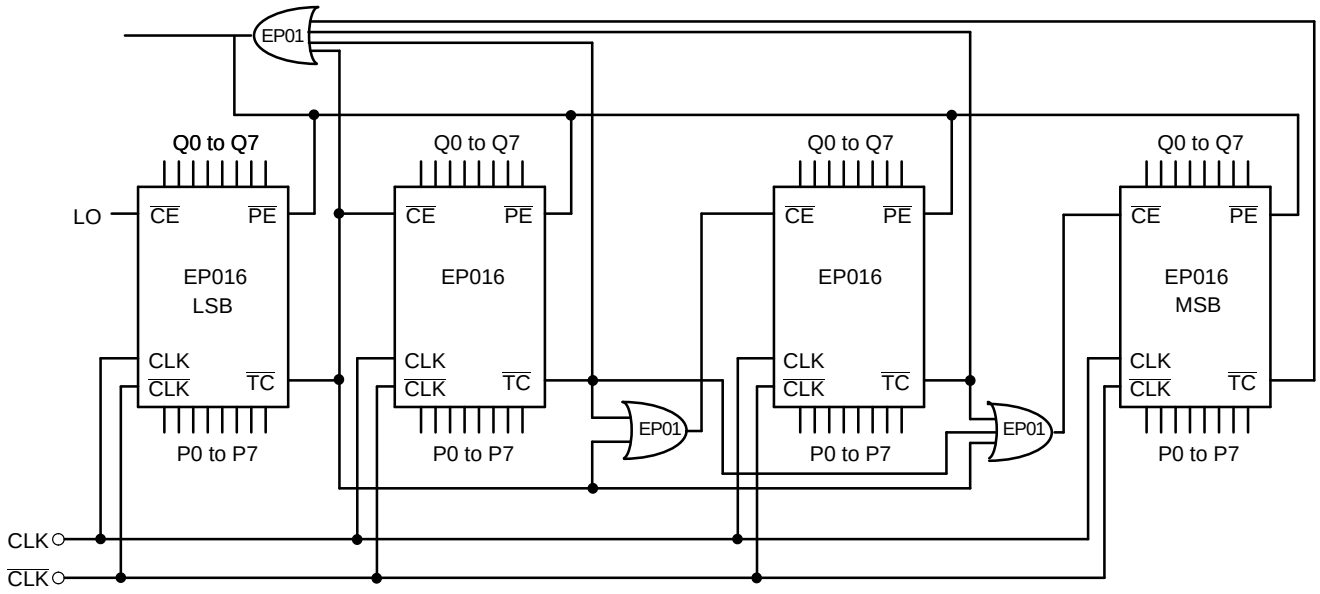


Figure 7. 32-Bit Cascaded EP016A Programmable Divider

Figure 7 shows a typical block diagram of a 32-bit divider chain. Once again to maximize the frequency of operation EP01 OR gates were used. For lower frequency applications a slower OR gate could replace the EP01. Note that for a 16-bit divider the OR function feeding the $\overline{PE}$ (program enable) input CANNOT be replaced by a wire OR tie as the $\overline{TC}$ output of the least significant EP016A must also feed the $\overline{CE}$ input of the most significant EP016A. If the two $\overline{TC}$ outputs were OR tied the cascaded count operation would not operate properly. Because in the cascaded form the $\overline{PE}$ feedback is external and requires external gating, the maximum frequency of operation will be significantly less than the same operation in a single device.

ORDERING INFORMATION

Device	Package	Shipping†
MC100EP016AFAG	LQFP−32 (Pb−Free)	250 Units / Tray
MC100EP016AMNG	QFN−32 (Pb−Free)	74 Units / Rail
MC100EP016AMNR4G	QFN−32 (Pb−Free)	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Resource Reference of Application Notes

AN1405/D − ECL Clock Distribution Techniques

AN1406/D − Designing with PECL (ECL at +5.0 V)

AN1503/D − ECLinPS™ I/O SPiCE Modeling Kit

AN1504/D − Metastability and the ECLinPS Family

AN1568/D − Interfacing Between LVDS and ECL

AN1672/D − The ECL Translator Guide

AND8001/D − Odd Number Counters Design

AND8002/D − Marking and Date Codes

AND8020/D − Termination of ECL Logic Devices

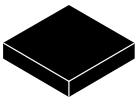
AND8066/D − Interfacing with ECLinPS

AND8090/D − AC Characteristics of ECL Devices

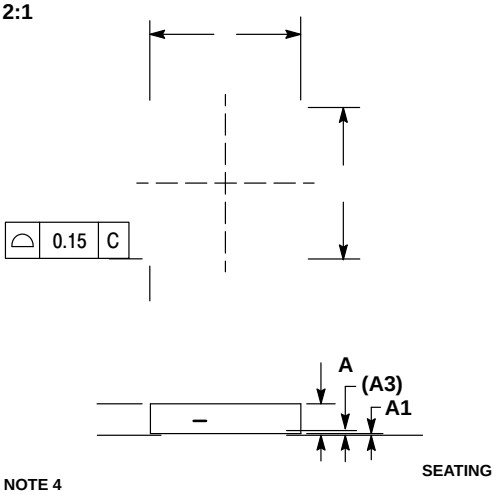
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

QFN32 5x5, 0.5P
CASE 488AM
ISSUE A

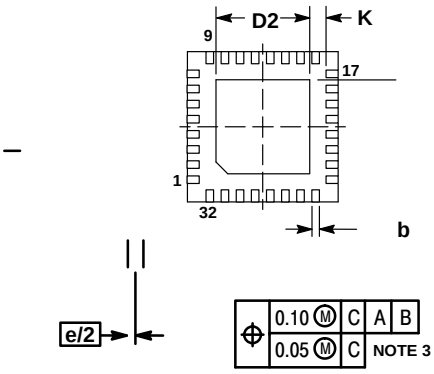
DATE 23 OCT 2013



SCALE 2:1



	MIN	MAX
A	0.80	1.00
A1	---	0.05
A3	0.20 REF	
b	0.18	0.30
D	5.00 BSC	
D2	2.95	3.25
E	5.00 BSC	
E2	2.95	3.25
e	0.50 BSC	
K	0.20	---
L	0.30	0.50
L1	---	0.15



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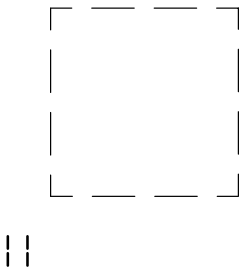

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LQFP−32, 7x7
CASE 561AB
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