3.3 V/5 V ECL Quad 4-Input OR/NOR

MC100EP101

Description

The MC100EP101 is a Quad 4−input OR/NOR gate. The device is functionally equivalent to the E101. With AC performance faster than the E101 device, the EP101 is ideal for applications requiring the fastest AC performance available.

The 100 Series contains temperature compensation.

Features

- 250 ps Typical Propagation Delay
- Maximum Frequency > 3 GHz Typical
- PECL Mode Operating Range: V_{CC} = 3.0 V to 5.5 V with V_{EE} = 0 V
- NECL Mode Operating Range: V_{CC} = 0 V with V_{EE} = −3.0 V to −5.5 V
- Open Input Default State
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

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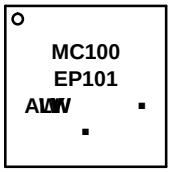
MARKING DIAGRAMS*

LQFP−32
FA SUFFIX
CASE 561AB

1 32

QFN32
MN SUFFIX
CASE 488AM

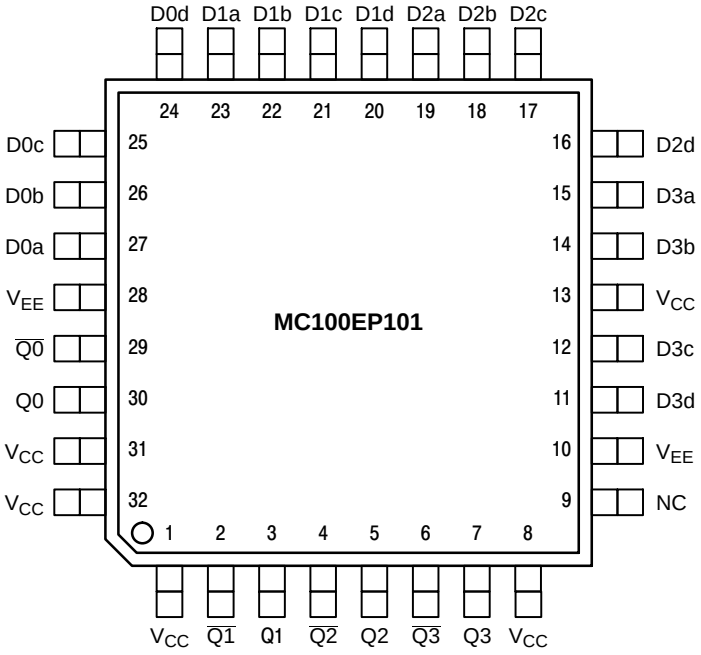


(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

Device	Package	Shipping
MC100EP101FAG	LQFP 32 (Pb Free)	250 Units / Tray
MC100EP101MNG	QFN 32 (Pb Free)	74 Units / Tube



Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. 32−Lead LQFP Pinout (Top View)

Table 1. PIN DESCRIPTION

PIN	FUNCTION
D0a* D3d*	ECL Data Inputs
Q0 Q3, $\overline{Q0}$ $\overline{Q3}$	ECL Data Outputs
V_{CC}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

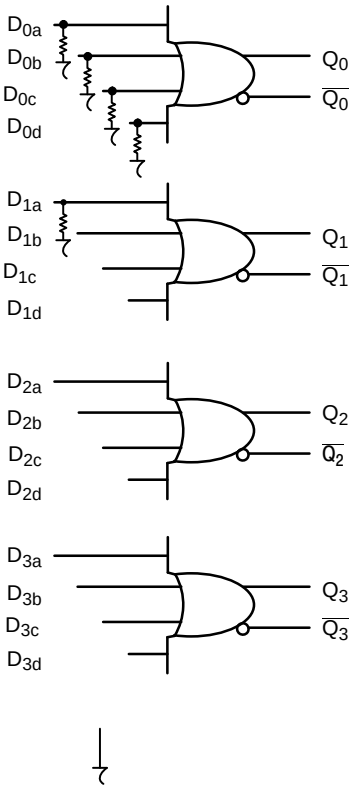


Table 2. TRUTH TABLE

Dna	Dnb	Dnc	Dnd	Qn	$\overline{Qn}$
L	L	L	L	L	H
H	X	X	X	H	L
X	H	X	X	H	L
X	X	H	X	H	L
X	X	X	H	H	L
H	H	H	H	H	L

Table 3. ATTRIBUTES

Characteristics	Value
Internal Input Pulldown Resistor	75 kΩ
Internal Input Pullup Resistor	N/A
ESD Protection Human Body Model Machine Model Charged Device Model	 > 4 kV > 100 V > 2 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)	Pb Free Pkg
LQFP 32 QFN 32	Level 2 Level 1
Flammability Rating Oxygen Index: 28 to 34	 UL 94 V 0 @ 0.125 in
Transistor Count	173 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		6	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		6	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \le V_{CC}$ $V_I \le V_{EE}$	6 6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			±0.5	mA
T_A	Operating Temperature Range			40 to +85	°C
T_{stg}	Storage Temperature Range			65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 lfpm 500 lfpm	32 LQFP 32 LQFP	80 55	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	Standard	32 LQFP	12 to 17	°C/W
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 lfpm 500 lfpm	QFN 32 QFN 32	31 27	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	2S2P	QFN 32	12	°C/W
T_{sol}	Wave Solder (Pb Free)			265	°C

Table 5. 100EP DC CHARACTERISTICS, PECL V_{CC} = 3.3 V, V_{EE} = 0 V (Note 2)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	40	55	75	40	58	75	45	60	85	mA
V_{OH}	Output HIGH Voltage (Note 3)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
V_{OL}	Output LOW Voltage (Note 3)	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV
V_{IH}	Input HIGH Voltage (Single Ended)	2075		2420	2075		2420	2075		2420	mV
V_{IL}	Input LOW Voltage (Single Ended)	1355		1675	1355		1675	1355		1675	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	150			150			150			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

2. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.3 V to 2.2 V.
3. All loading with 50 Ω to V_{CC} 2.0 V.

Table 6. 100EP DC CHARACTERISTICS, PECL V_{CC} = 5.0 V, V_{EE} = 0 V (Note 4)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	40	58	75	40	61	75	45	64	85	mA
V_{OH}	Output HIGH Voltage (Note 5)	3855	3980	4105	3855	3980	4105	3855	3980	4105	mV
V_{OL}	Output LOW Voltage (Note5)	3055	3180	3305	3055	3180	3305	3055	3180	3305	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3775		4120	3775		4120	3775		4120	mV
V_{IL}	Input LOW Voltage (Single Ended)	3055		3375	3055		3375	3055		3375	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	150			150			150			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

4. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +2.0 V to 0.5 V.
5. All loading with 50 Ω to V_{CC} 2.0 V.

Table 7. 100EP DC CHARACTERISTICS, NECL V_{CC} = 0 V, V_{EE} = 5.5 V to 3.0 V (Note 6)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current V_{CC} = 3.3V V_{CC} = 5.0 V	40 40	55 58	75 75	40 40	58 61	75 75	45 45	60 64	85 85	mA
I_{EE}	Power Supply Current	50	63	80	55	67	85	60	70	88	mA
V_{OH}	Output HIGH Voltage (Note 7)	1145	1020	895	1145	1020	895	1145	1020	895	mV
V_{OL}	Output LOW Voltage (Note 7)	1945	1820	1695	1945	1820	1695	1945	1820	1695	mV
V_{IH}	Input HIGH Voltage (Single Ended)	1225		880	1225		880	1225		880	mV
V_{IL}	Input LOW Voltage (Single Ended)	1945		1625	1945		1625	1945		1625	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	150			150			150			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

6. Input and output parameters vary 1:1 with V_{CC}.
7. All loading with 50 Ω to V_{CC} 2.0 V.

Table 8. AC CHARACTERISTICS V_{CC} = 0 V; V_{EE} = 3.0 V to 5.5 V or V_{CC} = 3.0 V to 5.5 V; V_{EE} = 0 V (Note 8)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Frequency (See Figure 4. F_{max}/JITTER)		> 3			> 3			> 3		GHz
t_{PLH}, t_{PHL}	Propagation Delay D to Q, $\overline{Q}$										ps
	10	125	225	325	150	250	370	170	300	420	
	100	180	280	380	200	300	400	250	320	450	
t_{SKEW}	Within Device Skew Q, $\overline{Q}$		15	50		20	50		20	50	ps
	Device to Device Skew (Note 9)			200			200			200	
t_{JITTER}	Cycle to Cycle Jitter (See Figure 4. F_{max}/JITTER)		0.2	< 1		0.2	< 1		0.2	< 1	ps
					120	170	220				

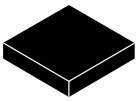
Resource Reference of Application Notes

AN1405/D	ECL Clock Distribution Techniques
AN1406/D	Designing with PECL (ECL at +5.0 V)
AN1503/D	ECLinPS™ I/O SPiCE Modeling Kit
AN1504/D	Metastability and the ECLinPS Family
AN1568/D	Interfacing Between LVDS and ECL
AN1672/D	The ECL Translator Guide
AND8001/D	Odd Number Counters Design
AND8002/D	Marking and Date Codes
AND8020/D	Termination of ECL Logic Devices
AND8066/D	Interfacing with ECLinPS
AND8090/D	AC Characteristics of ECL Devices

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

QFN32 5x5, 0.5P
CASE 488AM
ISSUE A

DATE 23 OCT 2013



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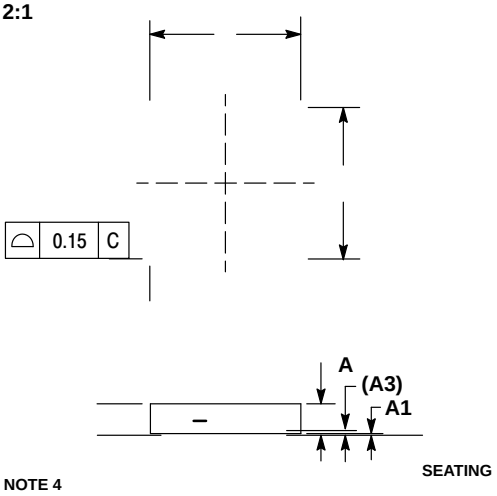
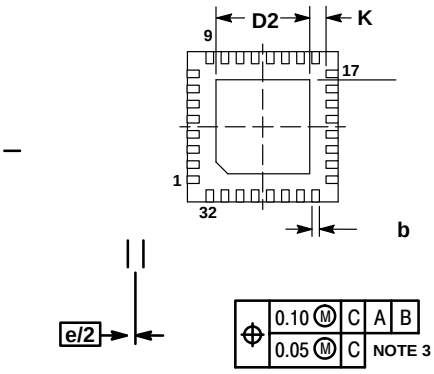


	MIN	MAX
A	0.80	1.00
A1	---	0.05
A3	0.20 REF	
b	0.18	0.30
D	5.00 BSC	
D2	2.95	3.25
E	5.00 BSC	
E2	2.95	3.25
e	0.50 BSC	
K	0.20	---
L	0.30	0.50
L1	---	0.15



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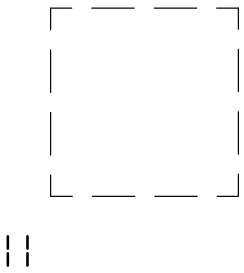

PITCH

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