

**3.3 V<sub>5</sub> V<sub>1:5</sub> ff <sup>n</sup>**  
**C / C / S C<sub>o</sub> ↓**

## Description

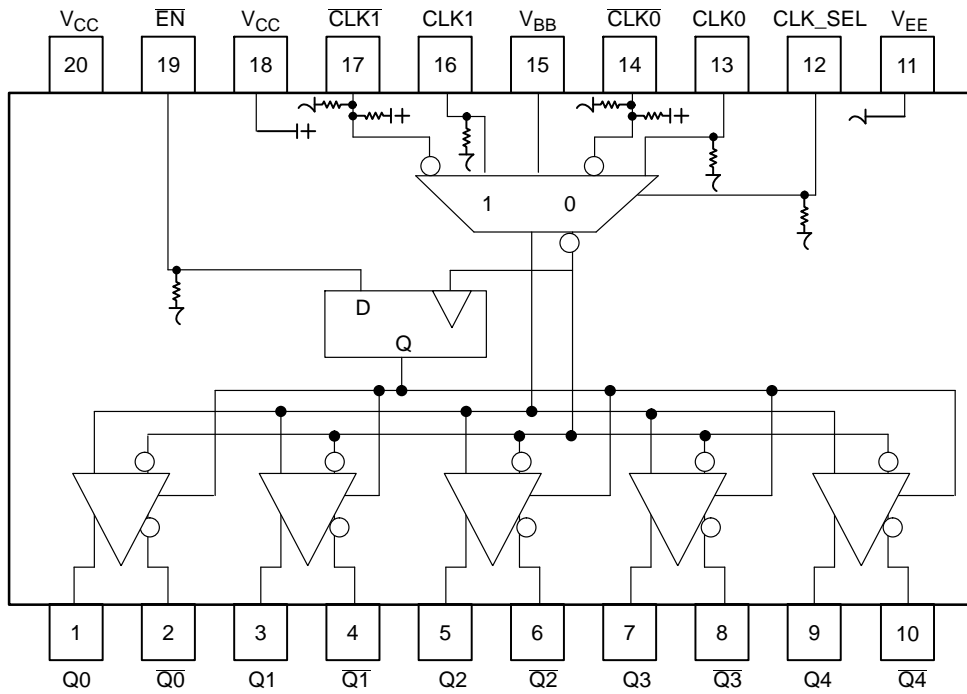
The MC100EP14 is a low skew 1-to-5 differential driver, designed with clock distribution in mind, accepting two clock sources into an input multiplexer. The ECL/PECL input signals can be either differential or single-ended (if the V<sub>BB</sub> output is used). HSTL inputs can be used when the LVEP14 is operating under PECL conditions.

The EP14 specifically guarantees low output-to-output skew. Optimal design, layout, and processing minimize skew within a device and from device to device.

To ensure that the tight skew specification is realized, both sides of any differential output need to be terminated even if only one output is being used. If an output pair is unused, both outputs may be left open (unterminated) without affecting skew.

The common enable ( $\overline{EN}$ ) is synchronous, outputs are enabled/disabled in the LOW state. This avoids a runt clock pulse when the device is enabled/disabled as can happen with an asynchronous control. The internal flip flop is clocked on the falling edge of the input clock,

# MC100EP14



**WARNING: All V<sub>CC</sub> and V<sub>EE</sub> pins must be externally connected to Power Supply to guarantee proper operation.**

**Figure 1. TSSOP-20 (Top View) and Logic Diagram**

**Table 1. PIN DESCRIPTION**

| Pin                                  | Function                           |
|--------------------------------------|------------------------------------|
| CLK0*, $\overline{\text{CLK0}}^{**}$ | ECL/PECL/HSTL CLK Input            |
| CLK1*, $\overline{\text{CLK1}}^{**}$ | ECL/PECL/HSTL CLK Input            |
| Q0:4, $\overline{\text{Q0}}:4$       | ECL/PECL Outputs                   |
| CLK_SEL*                             | ECL/PECL Active Clock Select Input |
| $\overline{\text{EN}}^*$             | ECL Sync Enable                    |
| V <sub>BB</sub>                      | Reference Voltage Output           |
| V <sub>CC</sub>                      | Positive Supply                    |
| V <sub>EE</sub>                      | Negative Supply                    |

\* Pins will default low when left open.

\*\* Pins will default to V<sub>CC</sub>/2 when left open.

**Table 2. FUNCTION TABLE**

| CLK0 | CLK1 | CLK_SEL | $\overline{\text{EN}}$ | Q  |
|------|------|---------|------------------------|----|
| L    | X    | L       | L                      | L  |
| H    | X    | L       | L                      | H  |
| X    | L    | H       | L                      | L  |
| X    | H    | H       | L                      | H  |
| X    | X    | X       | H                      | L* |

\* On next negative transition of CLK0 or CLK1

# MC100EP14

**Table 3. ATTRIBUTES**

| Characteristics   |   | Value                       |             |
|---|---|-----------------------------|-------------|
| Internal Input Pulldown Resistor                              |   | 75 kΩ                       |             |
| Internal Input Pullup Resistor                                |   | 37.5 kΩ                     |             |
| ESD Protection  | Human Body Model<br>Machine Model<br>Charged Device Model | > 4 kV<br>> 200 V<br>> 2 kV |             |
| Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1) |   | Pb Pkg                      | Pb-Free Pkg |
| TSSOP-8   |   | Level 1                     | Level 1     |
| Flammability Rating   | Oxygen Index: 28 to 34                                    | UL 94 V-0 @ 0.125 in        |             |
| Transistor Count  |   | 357 Devices                 |             |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test        |   |                             |             |

1. For additional information, see Application Note AND8003/D.

**Table 4. MAXIMUM RATINGS**

| Symbol           | Parameter  | Condition 1                                    | Condition 2  | Rating      | Unit         |
|------------------|--|--|--|-------------|--------------|
| V <sub>CC</sub>  | PECL Mode Power Supply                             | V <sub>EE</sub> = 0 V                          |  | 6           | V            |
| V <sub>EE</sub>  | NECL Mode Power Supply                             | V <sub>CC</sub> = 0 V                          |  | -6          | V            |
| V <sub>I</sub>   | PECL Mode Input Voltage<br>NECL Mode Input Voltage | V <sub>EE</sub> = 0 V<br>V <sub>CC</sub> = 0 V | V <sub>I</sub> ≤ V <sub>CC</sub><br>V <sub>I</sub> ≥ V <sub>EE</sub> | 6<br>-6     | V<br>V       |
| I <sub>out</sub> | Output Current                                     | Continuous<br>Surge                            |  | 50<br>100   | mA<br>mA     |
| I <sub>BB</sub>  | V <sub>BB</sub> Sink/Source                        |  |  | ± 0.5       | mA           |
| T <sub>A</sub>   | Operating Temperature Range                        |  |  | -40 to +85  | °C           |
| T <sub>stg</sub> | Storage Temperature Range                          |  |  | -65 to +150 | °C           |
| θ <sub>JA</sub>  | Thermal Resistance (Junction-to-Ambient)           | 0 lfpm<br>500 lfpm                             | TSSOP-20<br>TSSOP-20   | 140<br>100  | °C/W<br>°C/W |
| θ <sub>JC</sub>  | Thermal Resistance (Junction-to-Case)              | Standard Board                                 | TSSOP-20   | 23 to 41    | °C/W         |
| T <sub>sol</sub> | Wave Solder  | <2 to 3 sec @ 248°C                            |  | 265         | °C           |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

# MC100EP14

**Table 5. 100EP DC CHARACTERISTICS, PECL  $V_{CC} = 3.3\text{ V}$ ,  $V_{EE} = 0\text{ V}$  (Note 2)**

| Symbol |
|--------|
|--------|

# MC100EP14

**Table 7. 100EP DC CHARACTERISTICS, NECL**  $V_{CC} = 0\text{ V}$ ;  $V_{EE} = -5.5\text{ V}$  to  $-3.0\text{ V}$  (Note 8)

| Symbol   | Characteristic               | -40°C |     |     | 25°C |     |     | 85°C |     |     | Unit |
|----------|------------------------------|-------|-----|-----|------|-----|-----|------|-----|-----|------|
|          |                              | Min   | Typ | Max | Min  | Typ | Max | Min  | Typ | Max |      |
| $I_{EE}$ | Power Supply Current         | 45    | 55  | 65  | 48   | 58  | 68  | 52   | 62  | 72  | mA   |
| $V_{OH}$ | Output HIGH Voltage (Note 9) |       |     |     |      |     |     |      |     |     |      |

# MC100EP14

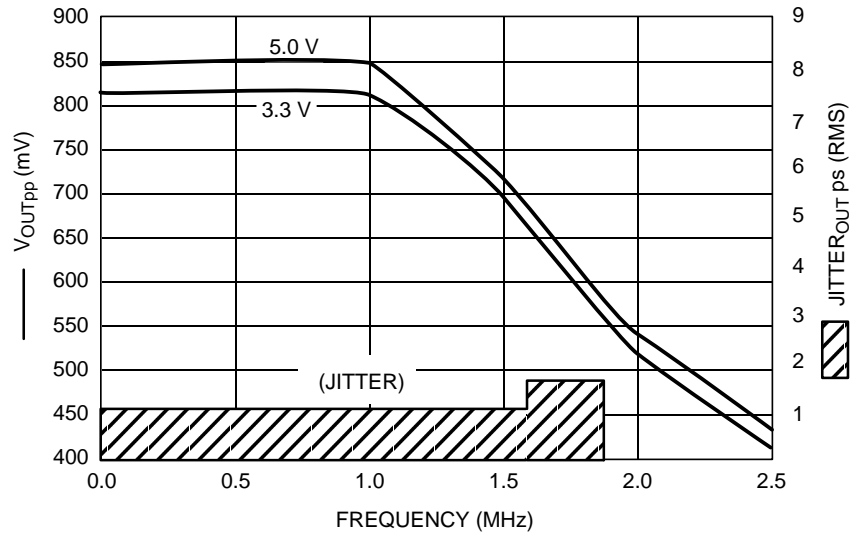


Figure 2. F<sub>max</sub>/Jitter

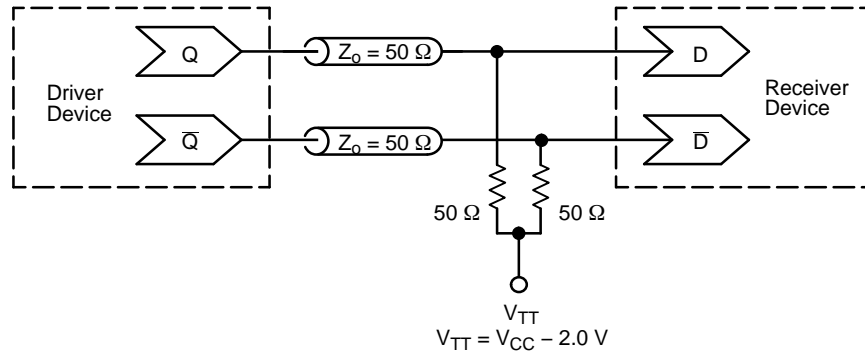


Figure 3. Typical Termination for Output Driver and Device Evaluation  
(See Application Note AND8020/D – Termination of ECL Logic Devices.)

## ORDERING INFORMATION

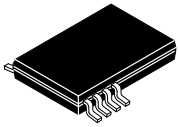
| Device |
|--------|
|--------|

3 ref3.4.SQB8 124.2142977

# MC100EP14

## Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPiCE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices



SCALE 2:1

**TSSOP-20 WB**  
CASE 948E  
ISSUE D

DATE 17 FEB 2016



**onsemi**, **onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi**

---

---