C100 14

3.3 V 5 V 1:5 ff n
C / C / S Co

Description

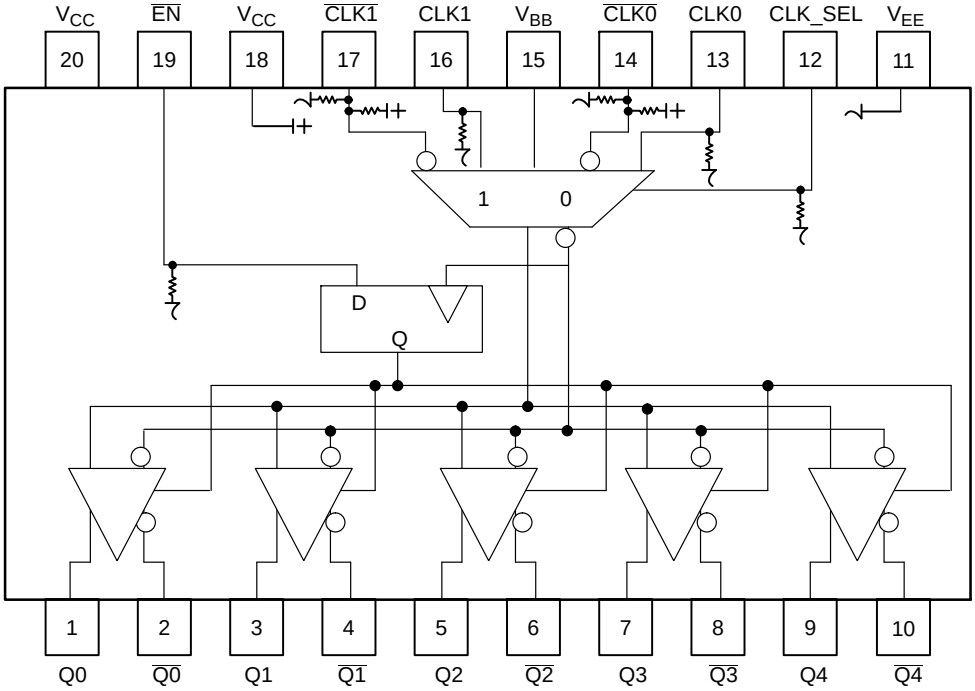
The MC100EP14 is a low skew 1−to−5 differential driver, designed with clock distribution in mind, accepting two clock sources into an input multiplexer. The ECL/PECL input signals can be either differential or single−ended (if the V_{BB} output is used). HSTL inputs can be used when the LVEP14 is operating under PECL conditions.

The EP14 specifically guarantees low output−to−output skew. Optimal design, layout, and processing minimize skew within a device and from device to device.

To ensure that the tight skew specification is realized, both sides of any differential output need to be terminated even if only one output is being used. If an output pair is unused, both outputs may be left open (unterminated) without affecting skew.

The common enable ($\overline{EN}$) is synchronous, outputs are enabled/ disabled in the LOW state. This avoids a runt clock pulse when the device is enabled/disabled as can happen with an asynchronous control. The internal flip flop is clocked on the falling edge of the input clock,

April, 2014 − Rev. 7
Publication Order Number:
MC100EP14/D



WARNING: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. TSSOP−20 (Top View) **and Logic Diagram**

Table 1. PIN DESCRIPTION

Pin	Function
CLK0*, $\overline{\text{CLK0}}$**	ECL/PECL/HSTL CLK Input
CLK1*, $\overline{\text{CLK1}}$**	ECL/PECL/HSTL CLK Input
Q0:4, $\overline{\text{Q0:4}}$	ECL/PECL Outputs
CLK_SEL*	ECL/PECL Active Clock Select Input
$\overline{\text{EN}}$*	ECL Sync Enable
V_{BB}	Reference Voltage Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply

* Pins will default low when left open.
** Pins will default to $V_{CC}/2$ when left open.

Table 2. FUNCTION TABLE

CLK0	CLK1	CLK_SEL	$\overline{\text{EN}}$	Q
L	X	L	L	L
H	X	L	L	H
X	L	H	L	L
X	H	H	L	H
X	X	X	H	L*

* On next negative transition of CLK0 or CLK1

Table 3. ATTRIBUTES

Characteristics		Value	
Internal Input Pulldown Resistor		75 kΩ	
Internal Input Pullup Resistor		37.5 kΩ	
ESD Protection	Human Body Model Machine Model Charged Device Model	> 4 kV > 200 V > 2 kV	
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)		Pb Pkg	Pb−Free Pkg
	TSSOP−8	Level 1	Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in	
Transistor Count		357 Devices	
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test			

1. For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		6	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		−6	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 −6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
T_A	Operating Temperature Range			−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm	TSSOP−20 TSSOP−20	140 100	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	Standard Board	TSSOP−20	23 to 41	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 5. 100EP DC CHARACTERISTICS, PECL V_{CC} = 3.3 V, V_{EE} = 0 V (Note 2)

Symbol

Table 7. 100EP DC CHARACTERISTICS, NECL V_{CC} = 0 V; V_{EE} = −5.5 V to −3.0 V (Note 8)

		−40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{EE}	Power Supply Current	45	55	65	48	58	68	52	62	72	mA
V_{OH}	Output HIGH Voltage (Note 9)										

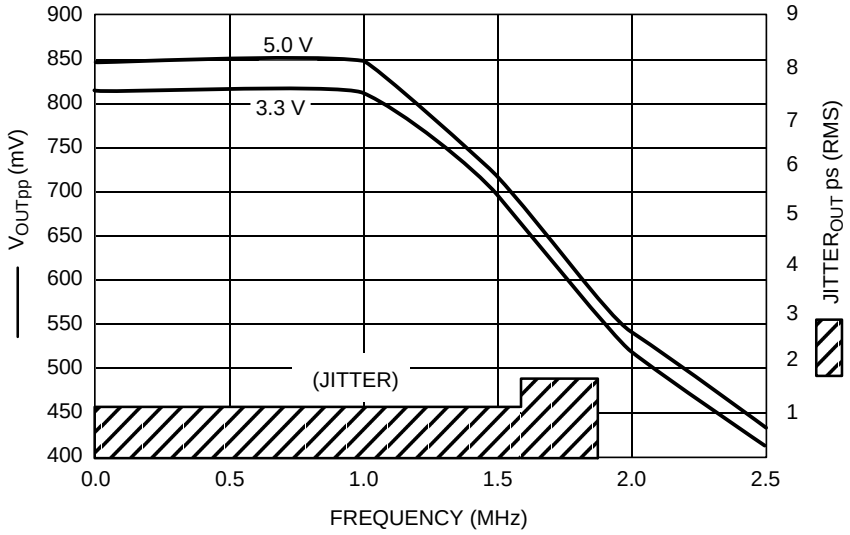


Figure 2. F_{max}/Jitter

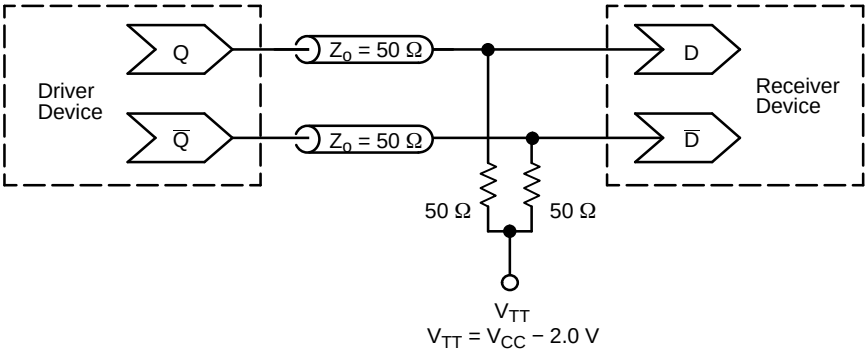


Figure 3. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D − Termination of ECL Logic Devices.)

ORDERING INFORMATION

Device			
	3	ref3.4.SQB8	124.2142977

Resource Reference of Application Notes

AN1405/D − ECL Clock Distribution Techniques

AN1406/D − Designing with PECL (ECL at +5.0 V)

AN1503/D − ECLinPS™ I/O SPiCE Modeling Kit

AN1504/D − Metastability and the ECLinPS Family

AN1568/D − Interfacing Between LVDS and ECL

AN1672/D − The ECL Translator Guide

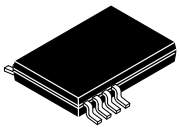
AND8001/D − Odd Number Counters Design

AND8002/D − Marking and Date Codes

AND8020/D − Termination of ECL Logic Devices

AND8066/D − Interfacing with ECLinPS

AND8090/D − AC Characteristics of ECL Devices



SCALE 2:1

TSSOP−20 WB
CASE 948E
ISSUE D

DATE 17 FEB 2016