MARKING

3.3 ECL -F _ D 0

MC100E 140

Description

The MC100EP140 is a three state phase frequency detector intended for phase locked loop applications which require a minimum amount of phase and frequency difference at lock. Since the part is designed with fully differential internal gates, the noise is reduced throughout the circuit, especially at high speeds. The basic operation of a Phase/Frequency Detector (PFD) is to "compare" an incoming signal (feedback) to a set reference signal. When the Reference (R) and Feedback (FB) inputs are unequal in frequency and/or phase, the differential UP (U) and DOWN (D) outputs will provide pulse streams which, when subtracted and integrated, provide an error voltage for control of a VCO. Detector states of operation are shown in the Figure 2 and the State Table.

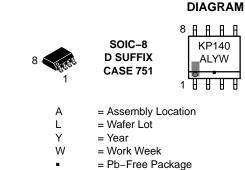
The typical output amplitude of the EP140 is 400 mV, allowing faster switching time and greater bandwidth. For proper operation, the input edge rate of the R and FB inputs should be less than 5 ns.

More information on Phase Lock Loop operation and application can be found in AND8040.

The pinout is shown in Figure 1, the logic diagram in Figure 3, and the typical termination in Figure 5.

Features

- 500 ps Typical Propagation Delay
- Maximum Frequency > 2.1 GHz Typical
- Fully Differential Internally
- Advanced High Band Output Swing of 400 mV
- Transfer Gain: 1.0 mV/Degree at 1.4 GHz 1.2 mV/Degree at 1.0 GHz
- Rise and Fall Time: 100 ps Typical
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: V_{CC} = 3.0 V to 3.6 V with V_{EE} = 0 V
- NECL Mode Operating Range: $V_{CC} = 0 V$ with $V_{EE} = 3.0 V$ to 3.6 V
- Open Input Default State
- These are Pb Free Devices



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

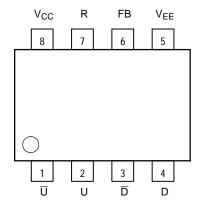


Figure 1. 8-Lead Pinout (Top View)

Table 1. PIN DESCRIPTION

PIN	FUNCTION
D, D	Differential Down Outputs
U, U	Differential Up Outputs
R*	ECL Reference Input
FB*	ECL Feedback Input
V _{CC}	Positive Supply
V _{EE}	Negative Supply

Table 2. STATE TABLE

PHASE DETECTOR STATE

Figure 2. Phase Detector Logic Model

Table 3. ATTRIBUTES

Characteristics	Value			
Internal Input Pulldown Resistor	75 k			

		-40°C			25°C			85°C			
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
I _{EE}	Power Supply Current	45	65	85	50	70	90	53	73	93	mA
V _{OH}	Output HIGH Voltage (Note 5)	-1075	-950	-825	-1025	-900	-775	-1000	-875	-750	mV
V _{OL}	Output LOW Voltage (Note 5)	-1525	-1400	-1275	-1500	-1375	-1250	-1475	-1350	-1225	mV
V _{IH}	Input HIGH Voltage (Single-Ended)	-1225		-880	-1225		-880	-1225		-880	mV
V _{IL}	Input LOW Voltage (Single-Ended)	-1945		-1625	-1945		-1625	-1945		-1625	mV
I _{IH}	Input HIGH Current			150			150			150	r

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Table 6. 100EP DC CHARACTERISTICS, NECL V_{CC} = 0 V, V_{EE} = –3.6 V to –3.0 V (Note 4)

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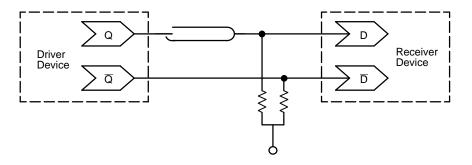
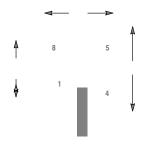


Figure 5. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D – Termination of ECL Logic Devices.)



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