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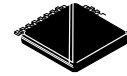
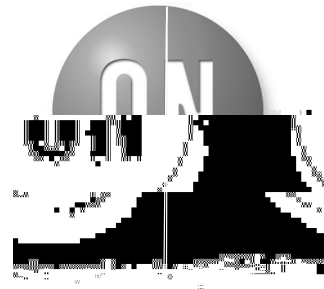
100 1 2

The MC100EP142 is a 9-bit shift register, designed with byte-parity applications in mind. The MC100EP142 is capable of performing serial/parallel data into serial/parallel out and shifting in only one direction. The nine inputs D0 – D8 accept parallel input data, while S-IN accepts serial input data. The Q0:87 outputs do not need to be terminated for the shift operation to function. To minimize power, any Q output not used should be left unterminated.

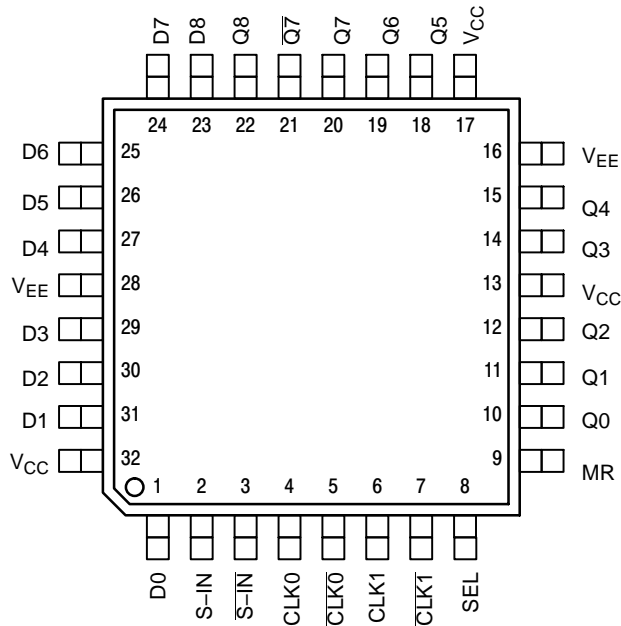
The SEL (Select) input pin is used to switch between the two modes of operation – SHIFT and LOAD. The shift direction is from Bit 0 to Bit 8. Input data is accepted by the registers a set-up time before the positive going edge of CLK0 or CLK1; shifting is also accomplished on the positive clock edge. A HIGH on the Master Reset pin (MR) asynchronously resets all the registers to zero, overriding CLK0 and CLK1 inputs.

The 100 Series contains temperature compensation.

- Shift Frequency >2.8 GHz (Typical)
- 9-Bit for Byte-Parity Applications
- Asynchronous Master Reset
- Dual Clocks
- PECL Mode Operating Range: $V_{CC} = 3.0\text{ V to }5.5\text{ V}$
with $V_{EE} = 0\text{ V}$
- NECL Mode Operating Range: $V_{CC} = 0\text{ V}$
with $V_{EE} = -3.0\text{ V to }-5.5\text{ V}$
- Open Input Default State
- Safety Clamp on Inputs
- These Devices are Pb-Free and are RoHS Compliant



*For additional marking information, refer to Application Note [AND8002/D](#).

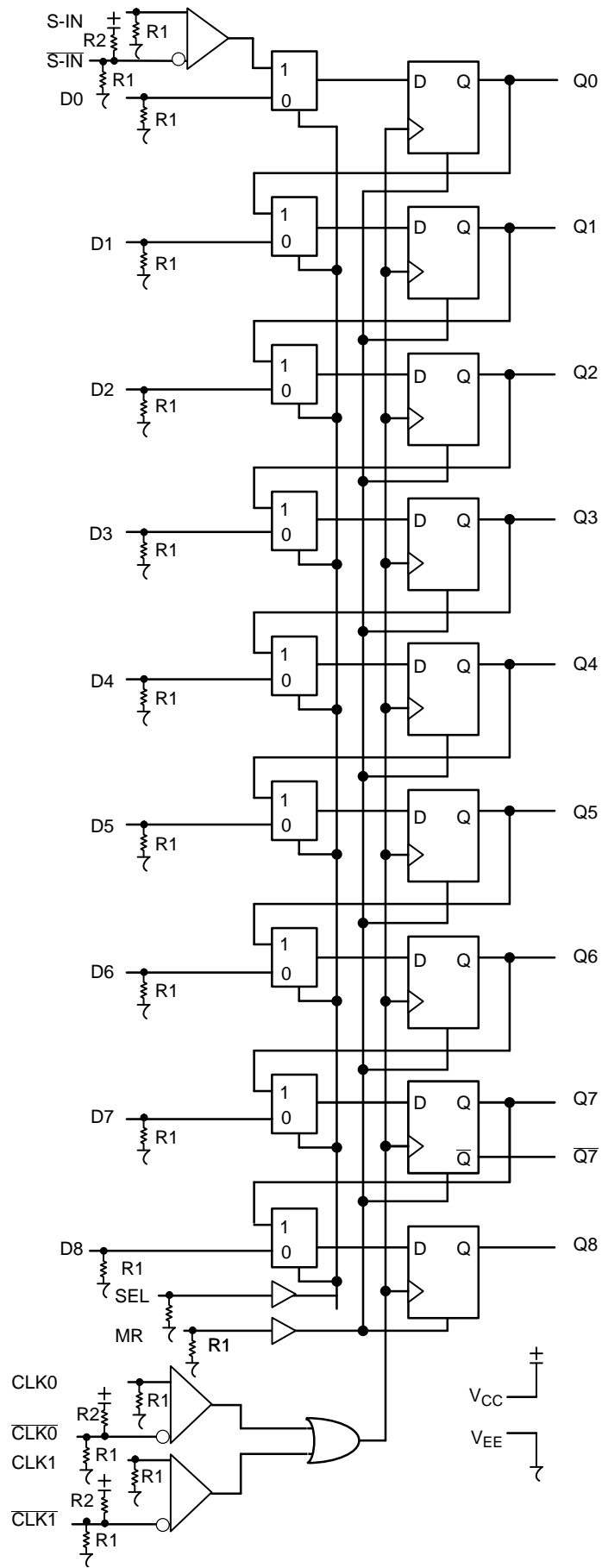


(Top View)

1,31,30,29,27,26,25,24,23	D[0:8]	ECL Input	Low	Single-Ended Parallel Data Inputs [0:8]. Internal 75 kΩ to V _{EE} .
2	S-IN	ECL Input	Low	Noninverted Differential Serial Input. Internal 75 kΩ to V _{EE} .
3	\overline{S} -IN	ECL Input	High	Inverted Differential Serial Input. Internal 75 kΩ to V _{EE} and 36.5 kΩ to V _{CC} .
4	CLK0	ECL Input	Low	Noninverted Differential CLK0 Input. Internal 75 kΩ to V _{EE} .
5	\overline{CLK} 0	ECL Input	High	Inverted Differential CLK0B Input. Internal 75 kΩ to V _{EE} and 36.5 kΩ to V _{CC} .
6	CLK1	ECL Input	Low	Noninverted Differential CLK1 Input. Internal 75 kΩ to V _{EE} .
7	\overline{CLK} 1	ECL Input	High	Inverted Differential CLK1B Input. Internal 75 kΩ to V _{EE} and 36.5 kΩ to V _{CC} .
8	SEL	ECL Input	Low	Single-Ended Select Logic Input. Internal 75 kΩ to V _{EE} .
9	MR	ECL Input	Low	Single-Ended Master Reset Logic Input. Internal 75 kΩ to V _{EE} .
10,11,12,14,15,18,19,22	Q0,Q1,Q2,Q3,Q4,Q5,Q6,Q8	ECL Output	–	Single-Ended parallel Data outputs [0,1,2,3,4,5,6,8]. Typically Terminated with 50 Ω to V _{TT} = V _{CC} – 2 V.
13,17,32	V _{CC}	–	–	Positive supply Voltage. All V _{CC} Pins must be Externally Connected to Power Supply to Guarantee Proper Operation.
16,28	V _{EE}	–	–	Negative supply Voltage. All V _{EE} Pins must be Externally connected to Power Supply to Guarantee Proper Operation.
20	Q7	ECL Output	–	Noninverted Differential parallel/Serial Data Output 7. Typically Terminated with 50 Ω to V _{TT} = V _{CC} – 2 V.
21	\overline{Q} 7	ECL Output	–	Inverted Differential parallel/Serial Data Output 7. Typically Terminated with 50 Ω to V _{TT} = V _{CC} – 2 V.

1. All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

(Note 2)															
	L	X	L	Z	Z	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9
	H	L	L	Z	Z	L	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
	H	H	L	Z	Z	H	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
	X	X	H	Z	Z	L	L	L	L	L					



Internal Input Pulldown Resistor (R1)

$V_{CC} = 3.3\text{ V}$, $V_{EE} = 0\text{ V}$ (Note 4)

I_{EE}	Negative Power Supply Current	105								

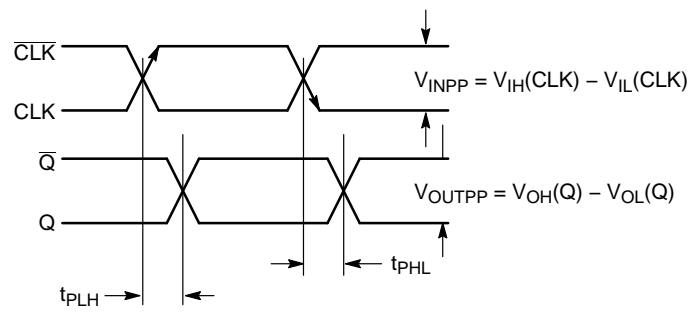


$V_{CC} = 5.0\text{ V}$, $V_{EE} = 0\text{ V}$ (Note 7)



V_{CC} = 3.0 V to 5.5 V; V_{EE} = 0.0 V or V_{CC} = 0.0 V; V_{EE} = -3.0 V to -5.5 V (Note 15)

		°			°			°				
f _{SHIFT}	Maximum Shift Frequency					2.8					GHz	
t _{PLH} , t _{PHL}	Propagation Delay to Output	CLKx MR	500 500	625 625	750 750	550 550	675 675	800 800	575 575	700 700	825 825	ps
t _s	Setup Time	D SEL	50 100	-50 50		50 100	-50 50		50 100	-50 50		ps
t _h	Hold Time	D SEL	100 50	50 -50		100 50	50 -50		100 50	50 -50		ps
t _{RR}	Reset Recovery Time					800						ps
t _{pw}	Minimum Pulse Width					200						ps
t _{SKEW}	Within-Device Skew (Note 16) Duty Cycle Skew (Note 17)	Q, \bar{Q}		50 5.0	100 20		50 5.0	100 20		50 5.0	100 20	ps
t _{JITTER}	Random Clock Jitter (Figure 3)			1	2		1					



LQFP-32, 7x7
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