3.3 V ECL Programmable Delay Chip

MC100EP195

The MC100EP195 is a Programmable Delay Chip (PDC) designed primarily for clock deskewing and timing adjustment. It provides variable delay of a differential NECL/PECL input transition.

The delay section consists of a programmable matrix of gates and multiplexers as shown in the logic diagram, Figure 3. The delay increment of the EP195 has a digitally selectable resolution of about 10 ps and a net range of up to 10.2 ns. The required delay is selected by

June, 2021 − Rev. 20
Publication Order Number:
MC100EP195/D

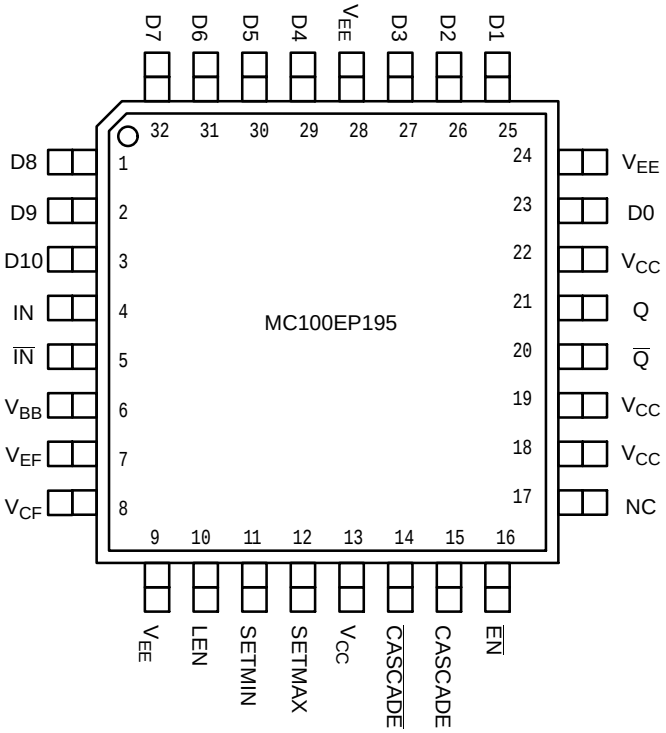


Figure 1. 32−Lead LQFP Pinout (Top View)

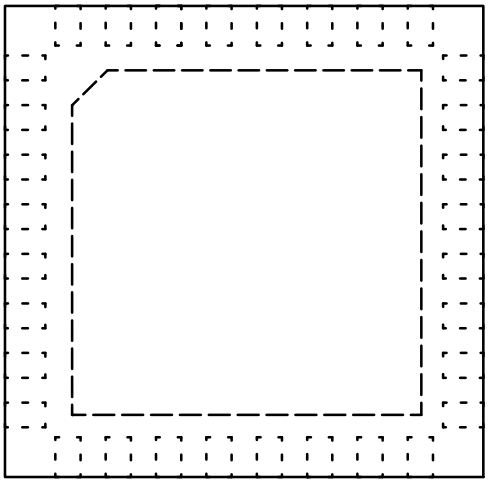


Table 1. PIN DESCRIPTION

Pin	Name	I/O	Default State	Description
23, 25, 26, 27, 29, 30, 31, 32, 1, 2	D[0:9]	LVCMOS, LVTTL, ECL Input	Low	Single−Ended Parallel Data Inputs [0:9]. Internal 75 kΩ to V_{EE}. (Note 1)
3	D[10]	LVCMOS, LVTTL, ECL Input	Low	Single−Ended CASCADE/$\overline{\text{CASCADE}}$ Control Input. Internal 75 kΩ to V_{EE}. (Note 1)
4	IN	ECL Input	Low	Noninverted Differential Input. Internal 75 kΩ to V_{EE}.
5	$\overline{\text{IN}}$	ECL Input	High	Inverted Differential Input. Internal 75 kΩ to V_{EE} and 36.5 kΩ to V_{CC}.
6	V_{BB}	−	−	ECL Reference Voltage Output
7	V_{EF}	−	−	Reference Voltage for ECL Mode Connection
8	V_{CF}	−	−	LVCMOS, ECL, OR LVTTL Input Mode Select
9, 24, 28	V_{EE}	−	−	Negative Supply Voltage. All V_{EE} Pins must be Externally Connected to Power Supply to Guarantee Proper Operation. (Note 2)
13, 18, 19, 22	V_{CC}	−	−	Positive Supply Voltage. All V_{CC} Pins must be externally Connected to Power Supply to Guarantee Proper Operation. (Note 2)
10	LEN	ECL Input	Low	Single−ended D pins LOAD / HOLD input. Internal 75 kΩ to V_{EE}.
11	SETMIN	ECL Input	Low	Single−

Table 2. CONTROL PIN

Pin	State	Function
EN	LOW (Note 3)	Input Signal is Propagated to the Output
	HIGH	Output Holds Logic Low State
LEN	LOW (Note 3)	Transparent or LOAD mode for real time delay values present on D[0:10].
	HIGH	LOCK and HOLD mode for delay values on D[0:10]; further changes on D[0:10] are not recognized and do not affect delay.
SETMIN	LOW (Note 3)	Output Delay set by D[0:10]
	HIGH	Set Minimum Output Delay
SETMAX	LOW (Note 3)	Output Delay set by D[0:10]
	HIGH	Set Maximum Output Delay
D10	LOW (Note 3)	CASCADE Output LOW, $\overline{\text{CASCADE}}$ Output HIGH
	HIGH	$\overline{\text{CASCADE}}$ Output LOW, CASCADE Output HIGH

3. Internal pulldown resistor will provide a logic LOW if pin is left unconnected.

Table 3. CONTROL D[0:10] INTERFACE

V_{CF}	V_{EF} Pin (Note 4)	ECL Mode
V_{CF}	No Connect	LVCMOS Mode
V_{CF}	1.5 V ±100 mV	LVTTL Mode (Note 5)

4. Short V_{CF} (pin 8) and V_{EF} (pin 7).
5. When Operating in LVTTL Mode, the reference voltage can be provided by connecting an external resistor, R_{CF} (suggested resistor value is 2.2 kΩ ±5%), between V_{CF} and V_{EE} pins.

Table 4. DATA INPUT ALLOWED OPERATING VOLTAGE MODE TABLE

POWER SUPPLY	CONTROL DATA SELECT INPUTS PINS (D [0:10])			
	LVCMOS	LVTTL	LVPECL	LVNECL
PECL Mode Operating Range	YES	YES	YES	N/A
NECL Mode Operating Range	N/A	N/A	N/A	YES

Table 5. ATTRIBUTES

Characteristics	Value
Internal Input Pulldown Resistor (R1)	75 kΩ
ESD Protection Human Body Model Machine Model Charged Device Model	 > 2 kV > 100 V > 2 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 6)	Pb

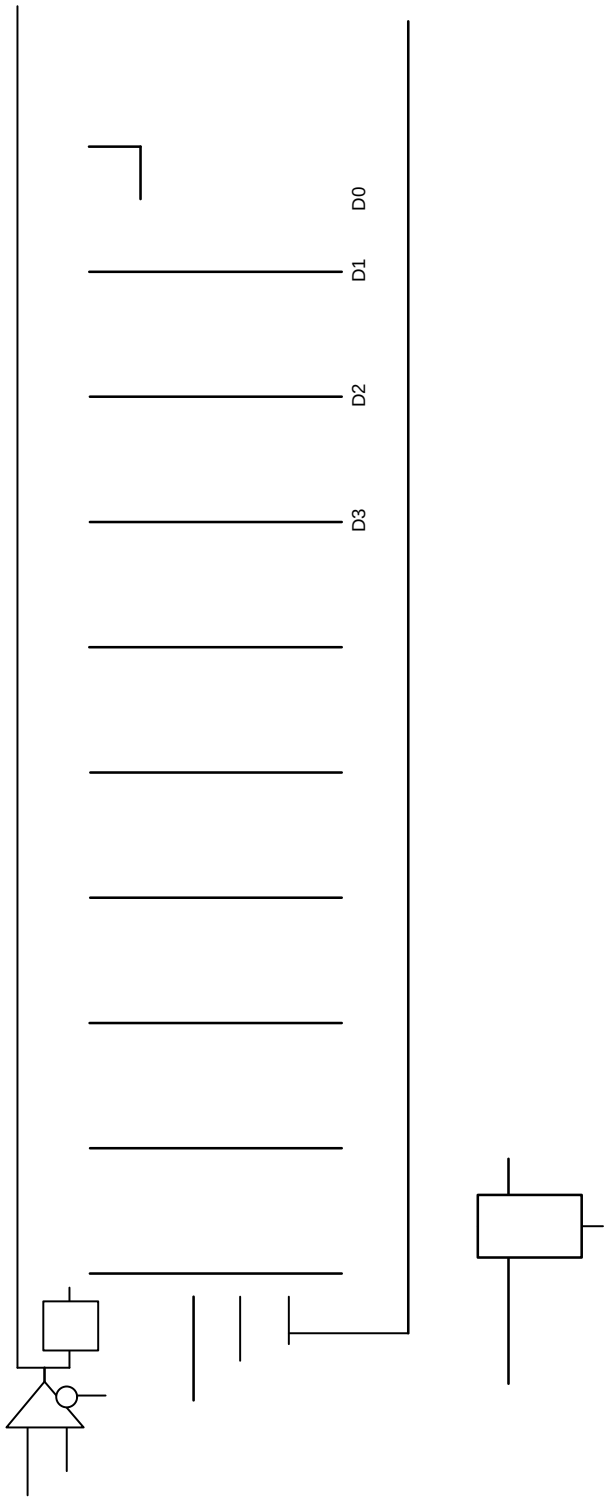

D0
D1
D2
D3

Table 6. THEORETICAL DELAY VALUES

D(9:0) Value	SETMIN	SETMAX	Programmable Delay*
XXXXXXXXXX	H	L	0 ps
0000000000	L	L	0 ps

Table 7. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V					

Table 8. 100EP DC CHARACTERISTICS, PECL V_{CC} = 3.3 V, V_{EE} = 0 V (Note 7)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Negative Power Supply Current	100	135	160	100	140	170	100	145	175	mA
V_{OH}	Output HIGH Voltage (Note 8)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
V_{OL}	Output LOW Voltage (Note 8)	1305	1480	1605	1305	1480	1605	1305	1480	1605	mV
V_{IH}	Input HIGH Voltage (Single−Ended) LVPECL CMOS TTL	 2075 2000 2000		 2420 3300 3300	 2075 2000 2000		 2420 3300 3300	 2075 2000 2000		 2420 3300 3300	mV
V_{IL}	Input LOW Voltage (Single−Ended) LVPECL CMOS TTL	 1305 0 0		 1675 800 800	 1305 0 0		 1675 800 800	 1305 0 0		 1675 800 800	mV
V_{BB}	ECL Output Voltage Reference	1775	1875	1975	1775	1875	1975	1775	1875	1975	mV
V_{CF}	LVTTL Mode Input Detect Voltage	1.4	1.5	1.6	1.4	1.5	1.6	1.4	1.5	1.6	V
V_{EF}	Reference Voltage for ECL Mode Connection	1920	2020	2120	1920	2020	2120	1920	2020	2120	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 9)	2.0		3.3	2.0		3.3	2.0		3.3	V
I_{IH}	Input HIGH Current (@ V_{IH})			150			150			150	μA
I_{IL}	Input LOW Current (@ V_{IL}) IN $\overline{IN}$	 0.5 −150			 0.5 −150			 0.5 −150			μA

V_{EE} = −3.3 V (Note 10)

			25°C			85°C			
		Max	Min	Typ	Max	Min	Typ	Max	Unit
		160	100	140	170	100	145	175	mA
		−895	−1145	−1020	−895	−1145	−1020	−895	mV
		−1695	−1995	−1820	−1695	−1995	−1820	−1695	mV
		−880	−1225		−880	−1225		−880	mV
		−1625	−1995		−1625	−1995		−1625	mV
		−1325	−1525	−1425	−1325	−1525	−1425	−1325	mV
		−1180	−1380	−1280	−1180	−1380			

Table 10. AC CHARACTERISTICS V_{CC} = 0 V; V_{EE} = −3.0 V to −3.6 V or V_{CC} = 3.0 V to 3.6 V; V_{EE} = 0 V (Note 14)

		−40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{max}	Maximum Frequency		1.2			1.2			1.2		GHz
t_{PLH} t_{PHL}	Propagation Delay IN to Q; D(0−10) = 0 IN to Q; D(0−10) = 1023 $\overline{EN}$ to Q; D(0−10) = 0 D0 to CASCADE	 1650 9500 1600 300	 2050 11500 2150 420	 2450 13500 2600 500	 1800 10000 1800 350	 2200 12200 2300 450	 2600 14000 2800 550	 1950 10800 2000 425	 2350 13300 2500 525	 2750 15800 3000 625	ps
t_{RANGE}	Programmable Range t_{PD} (max) − t_{PD} (min)	7850	9450		8200	10000		8850	10950		ps
Δt	Step Delay (Note 15) D0 High D1 High D2 High D3 High D4 High D5 High D6 High D7 High D8 High D9 High		 13 27 44 90 130 312 590 1100 2250 4500			 14 30 47 97 140 335 650 1180 2400 4800			 41 100 145 360 690 1300 2650 5300		ps
mono	Monotonicity (Note 21)					TBD					
t_{SKEW}	Duty Cycle Skew (Note 16) $\lvert t_{PHL} - t_{PLH} \rvert$		25			25			25		ps
t_s	Setup Time D to LEN D to IN (Note 17) $\overline{EN}$ to IN (Note 18)	 200 300 300	 0 140 150		 200 300 300	 0 160 170		 200 300 300	 0 180 180		ps
t_h	Hold Time LEN to D IN to $\overline{EN}$ (Note 19)	 200 400	 60 250		 200 400	 100 280		 200 400	 80 300		ps
t_R	Release Time $\overline{EN}$ to IN (Note 20) SET MAX to LEN SET MIN to LEN	 150 400 350	 −25 200 275		 150 400 350	 −75 250 200		 150 400 350	 −50 300 225		ps
t_{jitter}	RMS Random Clock Jitter @ 1.2 GHz IN to Q; D(0:10) = 0 or SETMIN IN to Q; D(0:10) = 1023 or SETMAX		 0.86 0.89			 1.16 1.09			 1.12 1.02		ps
V_{PP}	Input Voltage Swing (Differential Configuration)	150	800	1200							

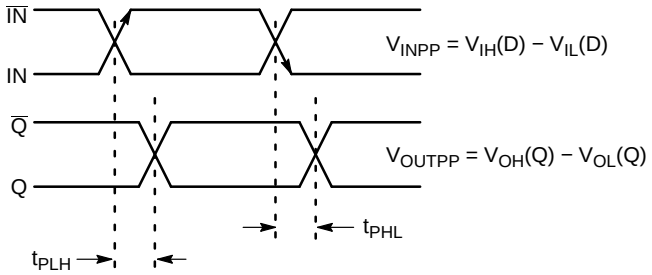


Figure 5. AC Reference Measurement

Cascading Multiple EP195s

To increase the programmable range of the EP195, internal cascade circuitry has been included. This circuitry allows for the cascading of multiple EP195s without the need for any external gating. Furthermore, this capability requires only one more address line per added E195. Obviously, cascading multiple programmable delay chips will result in a larger programmable range: however, this increase is at the expense of a longer minimum delay.

Figure 6 7[(allow Tf.8957.40007 Tc-8 0 058 T1 Tm0 g-0r)1ustrateslonge

An expansion of the latch section of the block diagram is pictured in Figure 7. Use of this diagram will simplify the explanation of how the cascade circuitry works. When D10 of chip #1 in Figure 6 is LOW this device's CASCADE output will also be low while the $\overline{\text{CASCADE}}$ output will be high. In this condition the SET MIN pin of chip #2 will be asserted HIGH and thus all of the latches of chip #2 will be reset and the device will be set at its minimum delay.

Chip #1, on the other hand, will have both SET MIN and SET MAX deasserted so that its delay will be controlled entirely by the address bus A0−A9. If the delay needed is greater than can be achieved with 1023 gate delays (1111111111 on the A0−A9 address bus) D10 will be asserted to signal the need to cascade the delay to the next EP195 device. When D10 is asserted, the SET MIN pin of chip #2 will be deasserted and SET MAX pin asserted resulting in the device delay to be the maximum delay. Table 11 shows the delay time of two EP195 chips in cascade.

To expand this cascading scheme to more devices, one simply needs to connect the D10 pin from the next chip to the address bus and CASCADE outputs to the next chip in the same manner as pictured in Figure 6. The only addition to the logic is the increase of one line to the address bus for cascade control of the second programmable delay chip.

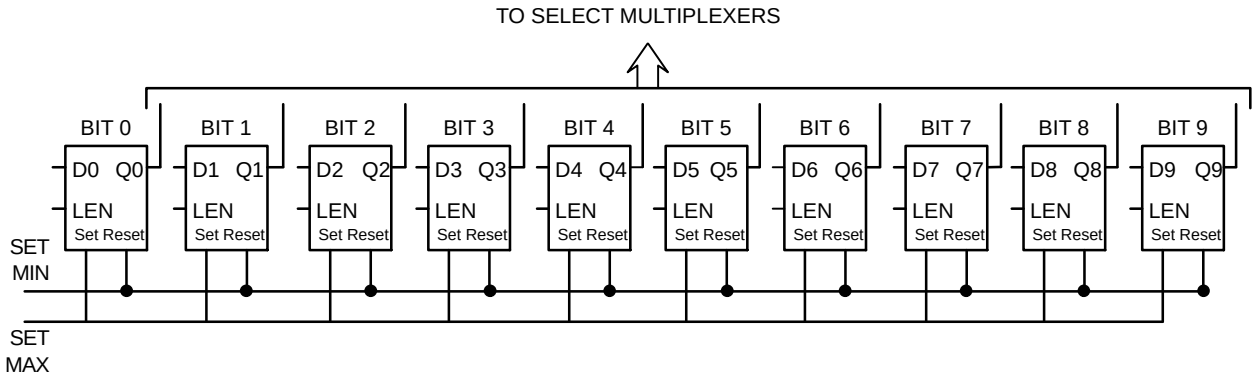


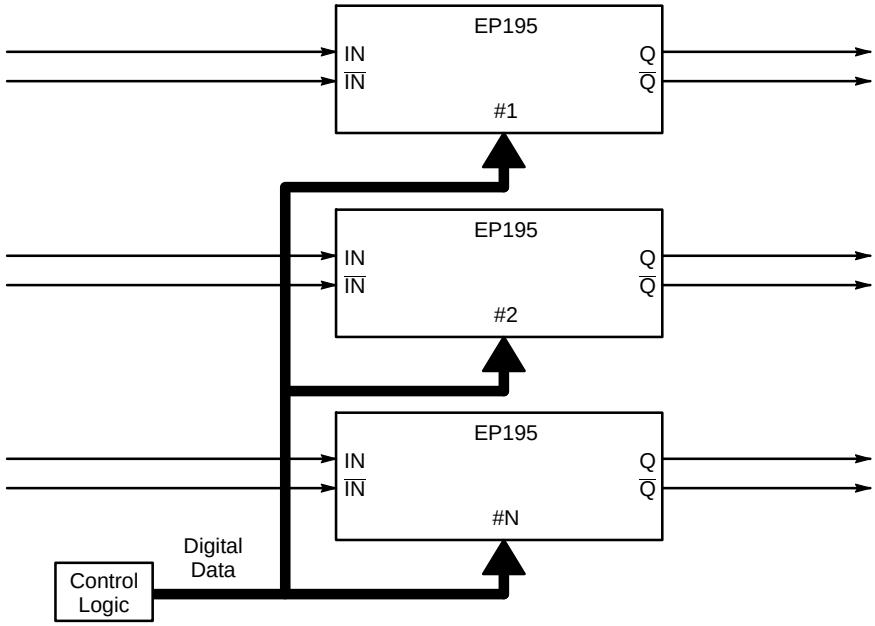
Figure 7. Expansion of the Latch Section of the EP195 Block Diagram

Table 11. Delay Value of Two EP195 Cascaded

VARIABLE INPUT TO CHIP #1 AND *SETMIN* FOR CHIP #2												
INPUT FOR CHIP #1												Total
D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Delay Value	Delay Value
0	0	0	0	0	0	0	0	0	0	0	0 ps	4400 ps
0	0	0	0	0	0	0	0	0	0	1	10 ps	4410 ps
0	0	0	0	0	0	0	0	0	1	0	20 ps	4420 ps
0	0	0	0	0	0	0	0	0	1	1	30 ps	4430 ps
0	0	0	0	0	0	0	0	1	0	0	40 ps	4440 ps
0	0	0	0	0	0	0	0	1	0	1	50 ps	4450 ps
0	0	0	0	0	0	0	0	1	1	0	60 ps	4460 ps
0	0	0	0	0	0	0	0	1	1	1	70 ps	4470 ps
0	0	0	0	0	0	0	1	0	0	0	80 ps	4480 ps
0	0	0	0	0	0	1	0	0	0	0	160 ps	4560 ps
0	0	0	0	0	1	0	0	0	0	0	220 ps	4720 ps
0	0	0	0	1	0	0	0	0	0	0		

Multi−Channel Deskewing

The most practical application for EP195 is in multiple channel delay matching. Slight differences in impedance and cable length can create large timing skews within a high−speed system. To deskew multiple signal channels, each channel can be sent through each EP195 as shown in Figure 8. One signal channel can be used as reference and the other EP195s can be used to adjust the delay to eliminate the timing skews. Nearly any high−speed system can be fine−tuned (as small as 10 ps) to reduce the skew to extremely tight tolerances.



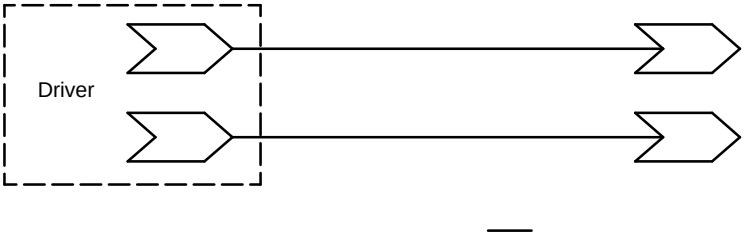


Figure 10. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D − Termination of ECL Logic Devices.)

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