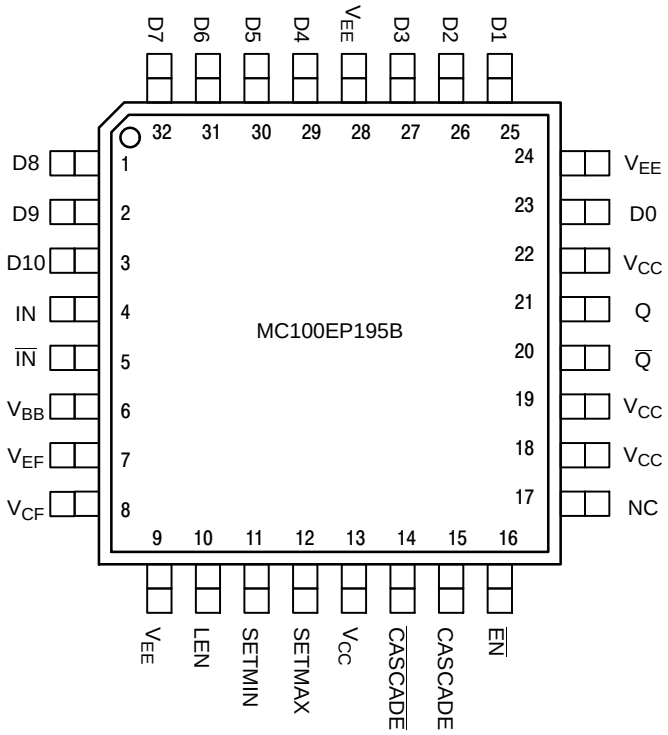


Figure 1. 32−Lead LQFP Pinout (Top View)

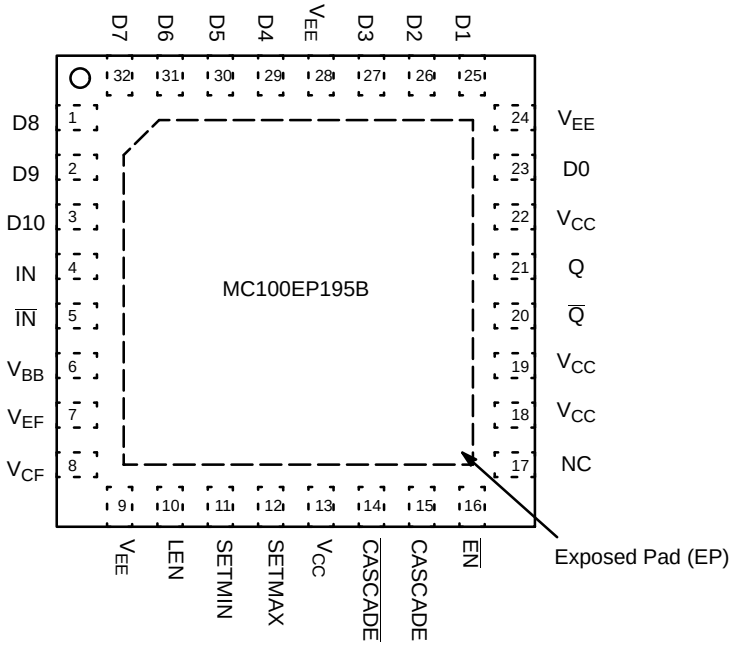


Figure 1. 32−Lead QFN (Top View)

Table 1. PIN DESCRIPTION

Pin	Name	I/O	Default State	Description
23, 25, 26, 27, 29, 30, 31, 32, 1, 2	D[0:9]	LVCMOS, LVTTL, ECL Input	Low	Single−Ended Parallel Data Inputs [0:9]. Internal 75 kΩ to V_{EE}. (Note 1)
3	D[10]	LVCMOS, LVTTL, ECL Input	Low	Single−Ended CASCADE/$\overline{\text{CASCADE}}$ Control Input. Internal 75 kΩ to V_{EE}. (Note 1)
4	IN	LVPECL, LVDS	Low	Noninverted Differential Input. Internal 75 kΩ to V_{EE}.
5	$\overline{\text{IN}}$	LVPECL, LVDS	High	Inverted Differential Input. Internal 75 kΩ to V_{EE} and 36.5 kΩ

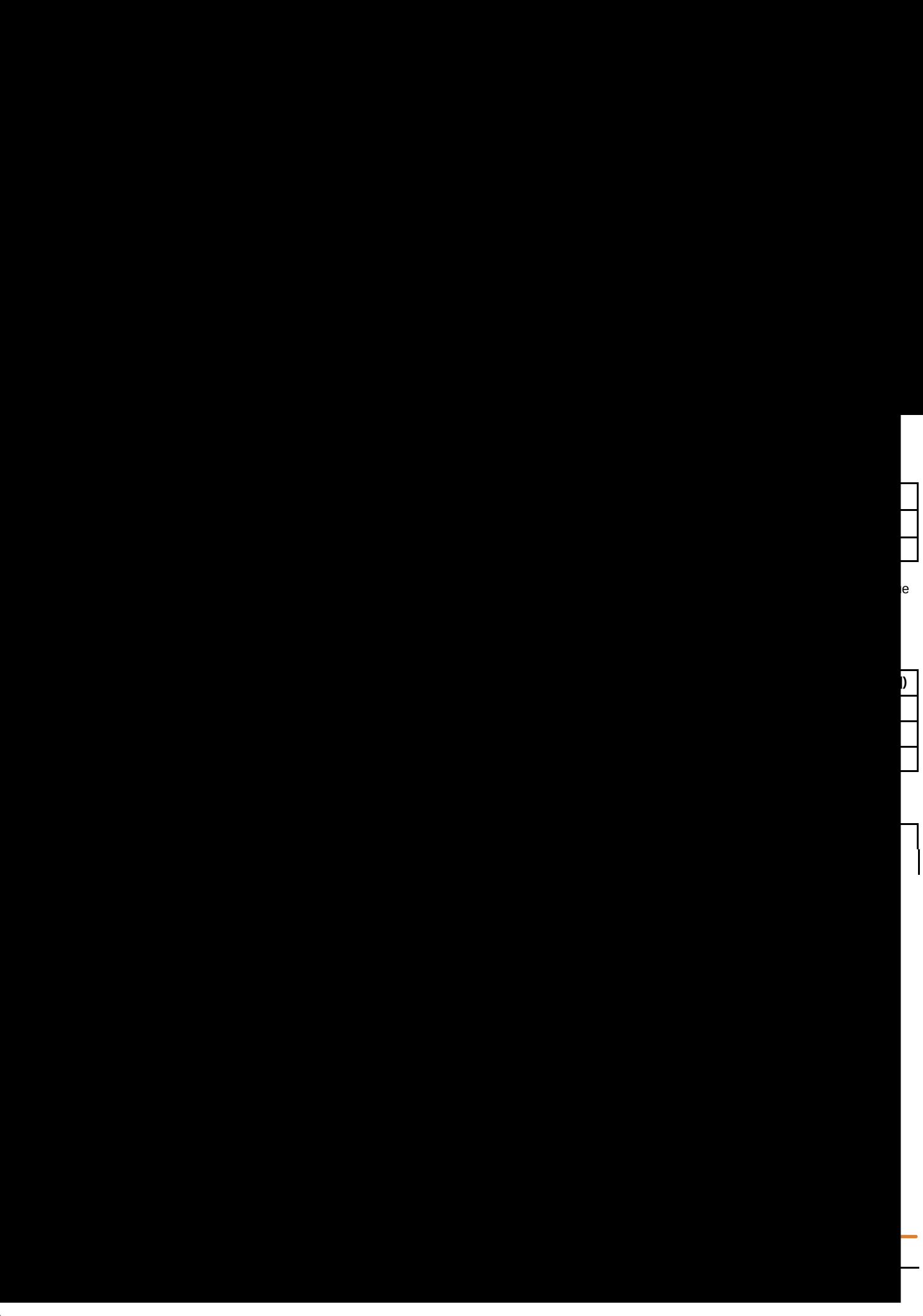


Table 6. THEORETICAL DELAY VALUES

D(9:0) Value	SETMIN	SETMAX	Programmable Delay*
XXXXXXXXXX	H	L	0 ps
0000000000	L	L	0 ps
0000000001	L	L	

rameter	Condition 1	Condition 2	Rating	Unit
upply	V_{EE} = 0 V		6	V
Supply	V_{CC} = 0 V		−6	V
tage ltage	V_{EE} = 0 V V_{CC} = 0 V	V_I V_{CC} V_I V_{EE}	6 −6	V V
	Continuous Surge		50 100	mA mA
			0.5	mA
Range			−40 to +85	C
ange			−65 to +150	C
nction−to−Ambient)	0 lfpm 500 lfpm	QFN−32 QFN−32	31 27	C/W C/W
nction−to−Case)	2S2P Standard Board	QFN−32	12	C/W
nction−to−Ambient)	0 lfpm 500 lfpm	LQFP−32 LQFP−32	80 55	C/W C/W
nction−to−Case)	2S2P Standard Board	LQFP−32	12 to 17	C/W
	<2 to 3 sec @ 260 C		265	C

e Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality
y occur and reliability may be affected.

TERISTICS, PECL (V_{CC} = 3.3 V, V_{EE} = 0 V) (Note 7)

	cteristic	−40 C			25 C			85 C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	Current	90	115	170	100	140	170	100	145	170	mA
	ote 8)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
	ote 8)	1305	1480	1605	1305	1480	1605	1305	1480	1605	mV
	gle−Ended)	2075 2000 2000		2420 3300 3300	2075 2000 2000		2420 3300 3300	2075 2000 2000		2420 3300 3300	mV
V_{IL}	Input LOW Voltage (Single−Ended) LVPECL CMOS TTL	1305 0 0		1675 800 800	1305 0 0		1675 800 800	1305 0 0		1675 800 800	mV
V_{BB}	ECL Output Voltage Reference	1775	1875	1975	1775	1875	1975	1775	1875	1975	mV

Table 9. 100EP DC CHARACTERISTICS, NECL

Table 10. AC CHARACTERISTICS (V_{CC} = 0 V; V_{EE} = −3.0 V to −3.6 V or V_{CC} = 3.0 V to 3.6 V; V_{EE} = 0 V) (Note 14) (continued)

		−40 C	25 C	85 C	

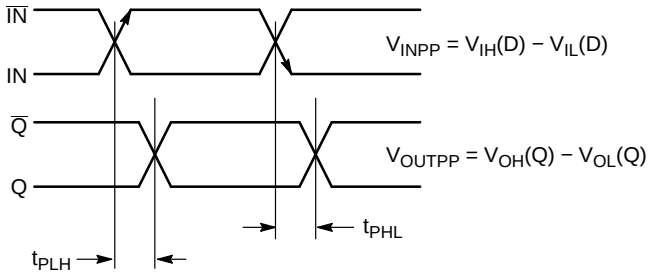
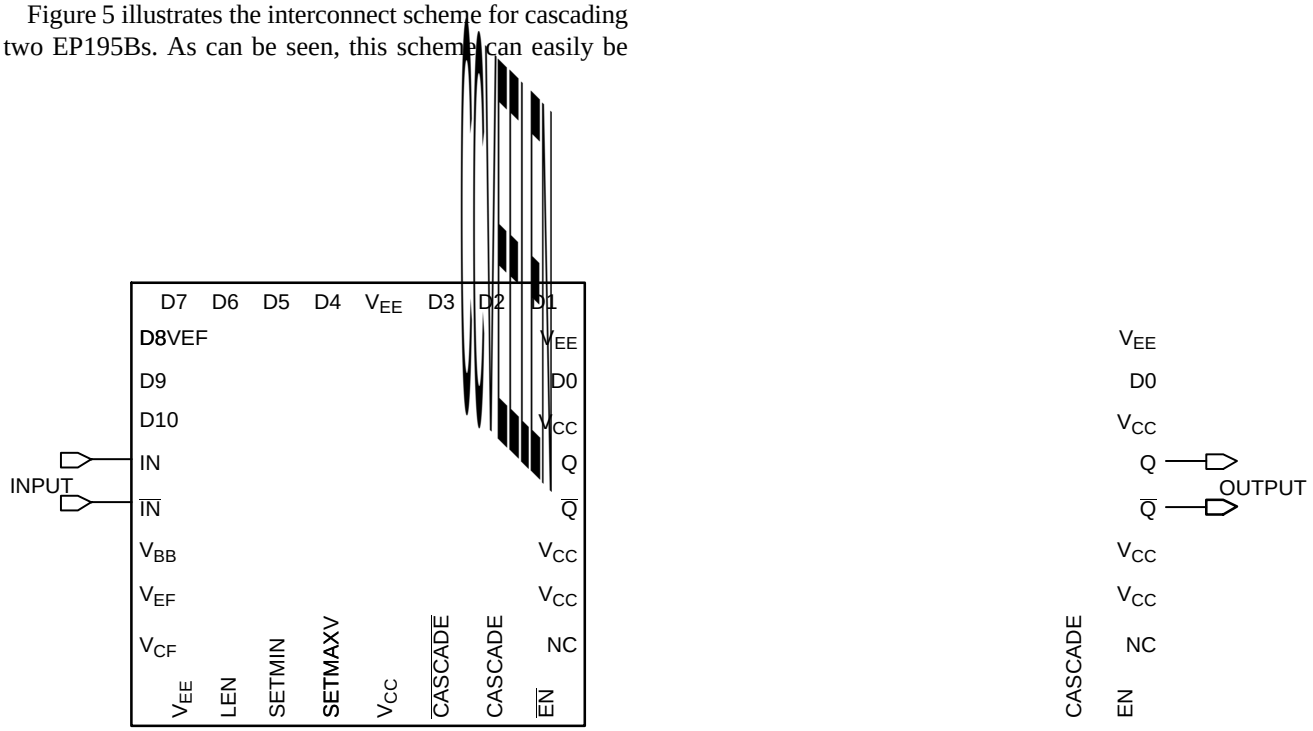


Figure 4. AC Reference Measurement

Cascading Multiple EP195Bs

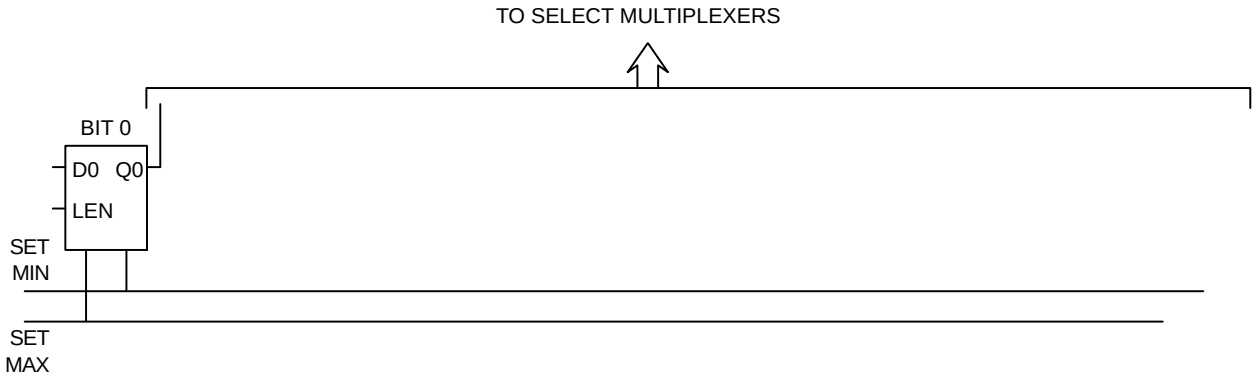
To increase the programmable range of the EP195B, internal cascade circuitry has been included. This circuitry allows for the cascading of multiple EP195Bs without the need for any external gating. Furthermore, this capability requires only one more address line per added E195B. Obviously, cascading multiple programmable delay chips will result in a larger programmable range: however, this increase is at the expense of a longer minimum delay.

Figure 5 illustrates the interconnect scheme for cascading two EP195Bs. As can be seen, this scheme can easily be expanded for larger EP195B chains. The D10 input of the EP195B is the CASCADE control pin. With the interconnect scheme of Figure 5 when D10 is asserted, it signals the need for a larger programmable range than is achievable with a single device and switches output pin CASCADE HIGH and pin $\overline{\text{CASCADE}}$ LOW. The A11 address can be added to generate a cascade output for the next EP195B. For a 2ĭdevice configuration, A11 is not required.



asserted to signal the need to cascade the delay to the next EP195B device. When D10 is asserted, the SET MIN pin of chip #2 will be deasserted and SET MAX pin asserted resulting in the device delay to be the maximum delay. Table 11 shows the delay time of two EP195B chips in cascade.

To expand this cascading scheme to more devices, one simply needs to connect the D10 pin from the next chip to the address bus and CASCADE outputs to the next chip in the same manner as pictured in Figure 5. The only addition to the logic is the increase of one line to the address bus for cascade control of the second programmable delay chip.



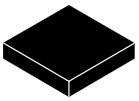
Multi−Channel Deskewing

The most practical application for EP195B is in multiple channel delay matching. Slight differences in impedance and cable length can create large timing skews within a high ĭspeed system. To deskew multiple signal channels, each channel can be sent through each EP195B as shown in Figure 7. One signal channel n

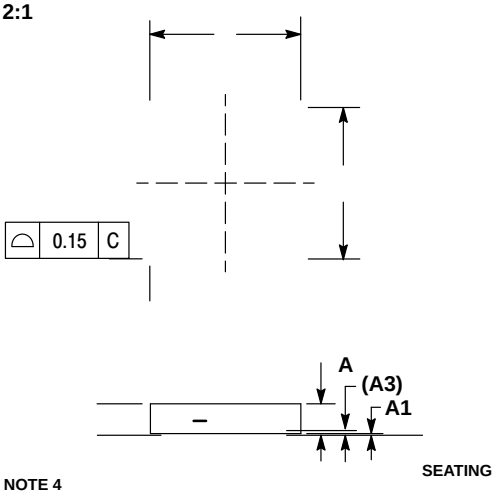
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

QFN32 5x5, 0.5P
CASE 488AM
ISSUE A

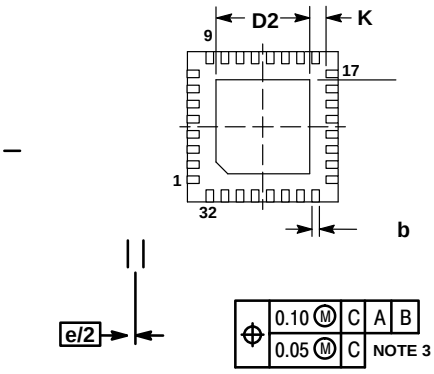
DATE 23 OCT 2013



SCALE 2:1

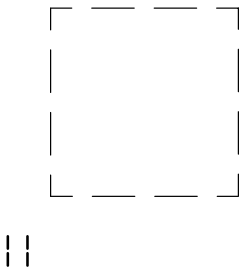


	MIN	MAX
A	0.80	1.00
A1	---	0.05
A3	0.20 REF	
b	0.18	0.30
D	5.00 BSC	
D2	2.95	3.25
E	5.00 BSC	
E2	2.95	3.25
e	0.50 BSC	
K	0.20	---
L	0.30	0.50
L1	---	0.15



XXXXXXXX
XXXXXXXX
AWLYYWW▪
▪Free indicator, “G” or

RECOMMENDED



PITCH

DIMENSION: MILLIMETERS

DOCUMENT NUMBER:	98AON20032D	

LQFP−32, 7x7
CASE 561AB
ISSUE O

DATE 19 JUN 200