

MC100EP196

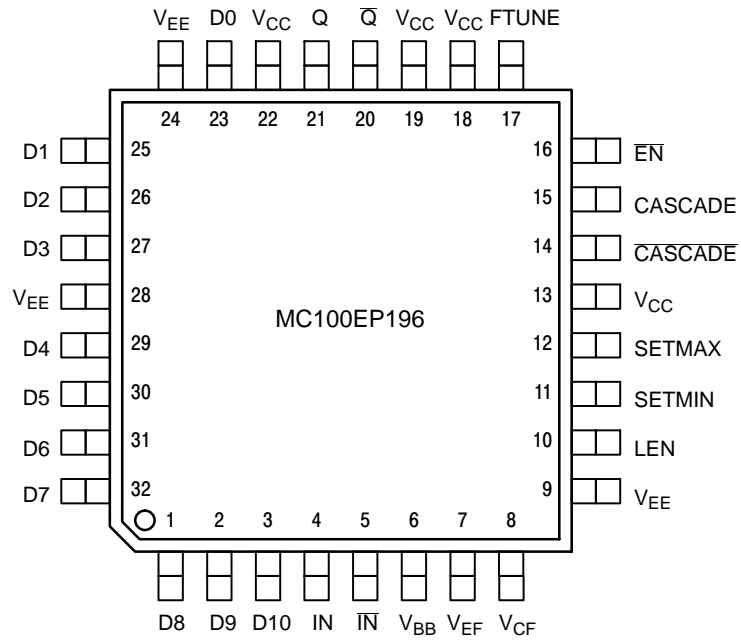


Figure 1. 32-Lead LQFP Pinout (Top View)

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Table 1. PIN DESCRIPTION

| Pin | Name | I/O | State | Description |
|--------------------------------------|-----------------|----------------------------|-------|--|
| 23, 25, 26, 27, 29, 30, 31, 32, 1, 2 | D[0:9] | LVC MOS, LV TTL, ECL Input | | Single-ended Parallel Data Inputs [0:9]. Internal 75 k Ω to V _{EE} . |
| 3 | D[10] | LVC MOS, LV TTL, ECL Input | LOW | Single-ended CASCADE/CASCADE Control Input. Internal to V _{EE} . (Note 1) |
| 4 | IN | ECL Input | LOW | Noninverted Differential Input. Internally Terminated with 50 Ω to V _{TT} = V _{CC} - 2 V. |
| 5 | IN | ECL Input | HIGH | Inverted Differential Input. Internal 75 k Ω to V _{EE} . |
| 6 | V _{BB} | - | - | ECL Reference Voltage Output |
| 7 | V _{EF} | - | - | Reference Voltage for ECL Mode Connection |
| 8 | V _{CF} | - | - | LVC MOS, ECL, OR LV TTL Input Mode Select |
| 9, 28 | V _{EE} | - | - | Negative Supply Voltage. All V _{EE} Pins must be Externally Connected to Power Supply to Guarantee Proper Operation. (Note 2) |
| 13, 18, 19, 22 | V _{CC} | - | - | Positive Supply Voltage. All V _{CC} Pins must be externally Connected to Power Supply to Guarantee Proper Operation. (Note 2) |
| 10 | LEN | ECL Input | | Single-ended Data Input Enable Pin. Internal 75 k Ω to V _{EE} . |
| 11 | SETMIN | ECL Input | | Single-ended Minimum Delay Set Logic Input. Internal 75 k Ω to V _{EE} . (Note 1) |
| 12 | SETMAX | ECL Input | LOW | Single-ended Maximum Delay Set Logic Input. Internal 75 k Ω to V _{EE} . (Note 1) |
| 14 | CASCADE | ECL Output | | Noninverted Differential Cascade Output. Typically Terminated with 50 Ω to V _{TT} = V _{CC} - 2 V. |
| 15 | CASCADE | ECL Output | | Noninverted Differential Cascade Output. Typically Terminated with 50 Ω to V _{TT} = V _{CC} - 2 V. |
| 16 | EN | ECL Input | | Single-ended Input Enable Pin. Internal 75 k Ω to V _{EE} . |
| 17 | FTUNE | Analog Input | | Frequency Tuning Input. |
| 21 | Q | ECL Output | | Noninverted Differential Output. Internally Terminated with 50 Ω to V _{TT} = V _{CC} - 2 V. |

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Table 2. CONTROL PIN

| Pin | State | Function |
|--------|--------------|--|
| EN | LOW (Note 3) | Input Signal is Propagated to the Output |
| | HIGH | Output Holds Logic Low State |
| LEN | LOW (Note 3) | Transparent or LOAD mode for real time delay values present on D[0:10]. |
| | HIGH | LOCK and HOLD mode for delay values on D[0:10]; further changes on D[0:10] are not recognized and do not affect delay. |
| SETMIN | LOW (Note 3) | Output Delay set by D[0:10] |
| | HIGH | Set Minimum Output Delay |
| SETMAX | LOW (Note 3) | Output Delay set by D[0:10] |
| | HIGH | Set Maximum Output Delay |
| D10 | LOW | CASCADE Output LOW, $\overline{\text{CASCADE}}$ Output HIGH |
| | HIGH | $\overline{\text{CASCADE}}$ Output LOW, CASCADE Output High |

3. Internal pulldown resistor will provide a logic LOW if pin is left unconnected.

Table 3. CONTROL D[0:10] INTERFACE

| Pin | State | Function |
|----------|----------------------------------|----------------------|
| V_{CF} | V_{EF} Pin (Note 4) | ECL Mode |
| V_{CF} | No Connect | LVC MOS Mode |
| V_{CF} | $1.5\text{ V} \pm 100\text{ mV}$ | LVTTTL Mode (Note 5) |

4. Short V_{CF} (pin 8) and V_{EF} (pin 7).

5. When Operating in LVTTTL Mode, the reference voltage can be provided by connecting an external resistor, R_{CF} (suggested resistor value is $2.2\text{ k}\Omega \pm 5\%$), between V_{CF} and V_{EE} pins.

Table 4. DATA INPUT ALLOWED OPERATING VOLTAGE MODE TABLE

| POWER SUPPLY | CONTROL DATA SELECT INPUTS PINS (D [0:10]) | | | |
|---------------------------|--|--------|--------|--------|
| | LVC MOS | LVTTTL | LVPECL | LVNECL |
| PECL Mode Operating Range | YES | YES | YES | N/A |
| NECL Mode Operating Range | N/A | N/A | | |

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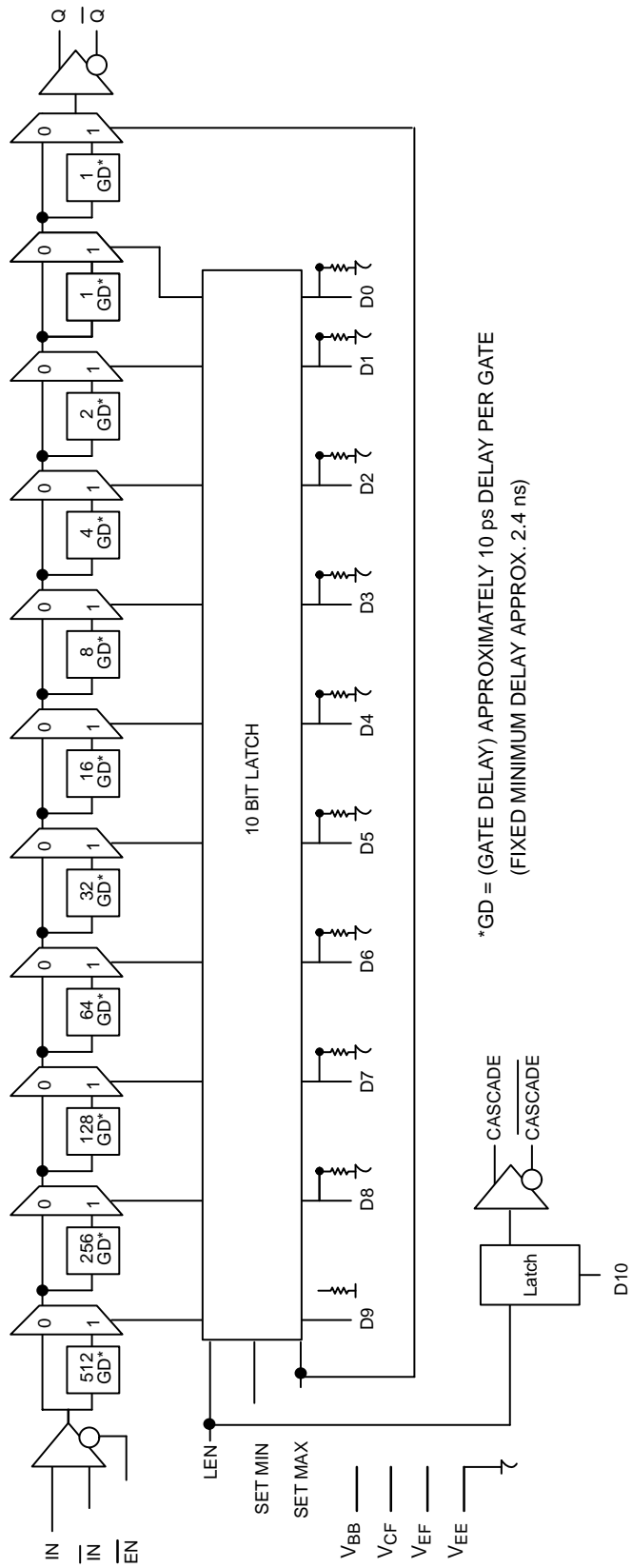


Figure 2. Logic Diagram

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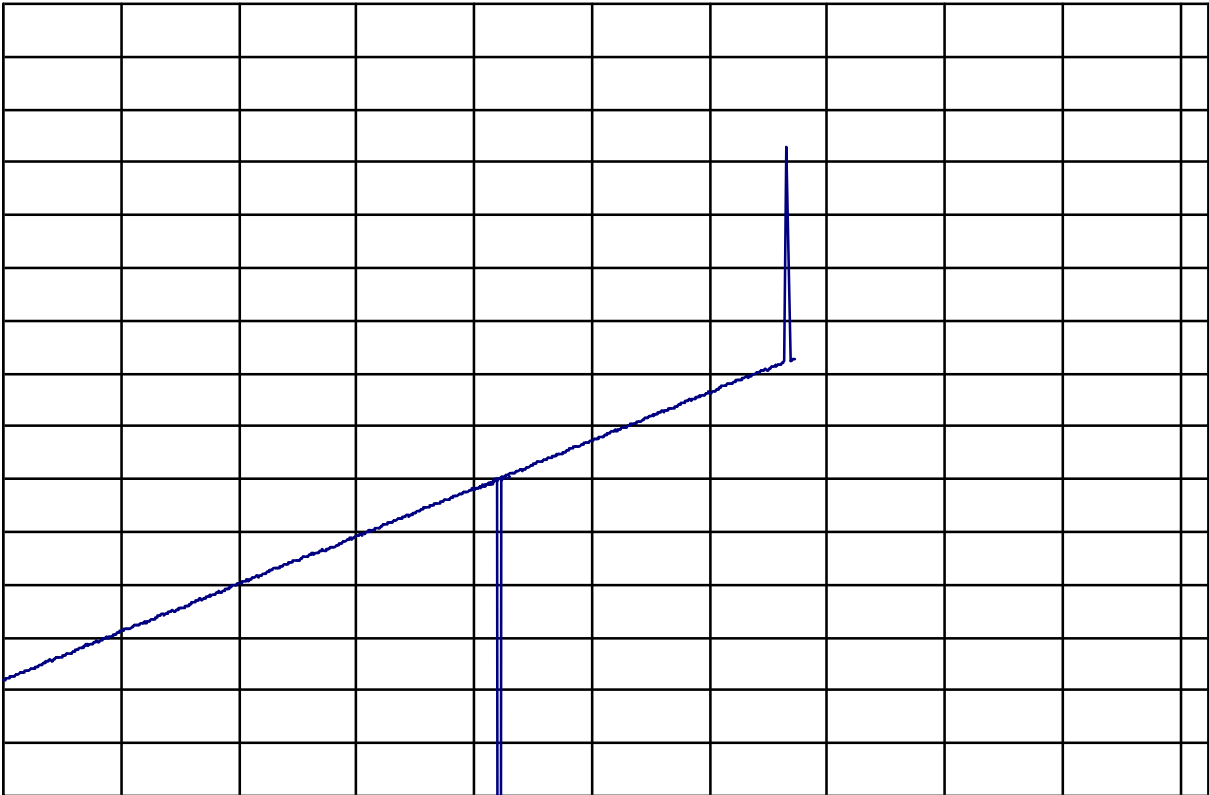
Table 5. THEORETICAL DELTA DELAY VALUES

| D(9:0) Value | SETMIN | SETMAX | Programmable Delay* |
|--------------|--------|--------|---------------------|
| XXXXXXXXXX | H | L | 0 ps |
| 000000000 | L | L | 0 ps |
| 000000001 | L | L | 10 ps |
| 000000010 | L | L | 20 ps |
| 000000011 | L | L | 30 ps |
| 000000100 | L | L | 40 ps |
| 000000101 | L | L | 50 ps |
| 000000110 | L | L | 60 ps |
| 000000111 | L | L | 70 ps |
| 000001000 | L | L | 80 ps |
| 000010000 | L | L | 160 ps |
| 000100000 | L | L | 320 ps |
| 001000000 | L | L | 640 ps |
| 010000000 | L | L | 1280 ps |
| 100000000 | L | L | 2560 ps |
| 100000000 | L | L | 5120 ps |
| 111111111 | L | L | 10230 ps |
| XXXXXXXXXX | L | H | 10240 ps |

*Fixed minimum delay not included.

Table 6. TYPICAL FTUNE DELAY PIN

| Input Range | Output Range |
|-----------------------|--------------|
| $V_{CC} - V_{EE}$ (V) | 0 – 60 (ps) |



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Table 8. MAXIMUM RATINGS

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Units |
|---------------|--|-----------------------|-------------------|-------------|-----------------------------|
| V_{CC} | PECL Mode Power Supply | $V_{EE} = 0\text{ V}$ | | 6 | V |
| V_{EE} | NECL Mode Power Supply | $V_{CC} = 0\text{ V}$ | | -6 | V |
| V_I | PECL Mode Input Voltage | $V_{EE} = 0\text{ V}$ | $V_I \leq V_{CC}$ | 6 | V |
| | NECL Mode Input Voltage | $V_{CC} = 0\text{ V}$ | $V_I \geq V_{EE}$ | -6 | V |
| I_{out} | Output Current | Continuous Surge | | 50 | mA |
| | | | | 100 | mA |
| I_{BB} | V_{BB} Sink/Source | | | ± 0.5 | mA |
| T_A | Operating Temperature Range | | | -40 to +85 | $^{\circ}\text{C}$ |
| T_{stg} | Storage Temperature Range | | | -65 to +150 | $^{\circ}\text{C}$ |
| θ_{JA} | Thermal Resistance (Junction-to-Ambient) | 0 lfpm | LQFP-32 | 80 | $^{\circ}\text{C}/\text{W}$ |
| | | 500 lfpm | LQFP-32 | 55 | $^{\circ}\text{C}/\text{W}$ |
| θ_{JC} | Thermal Resistance (Junction-to-Case) | Standard Board | LQFP-32 | 12 to 17 | $^{\circ}\text{C}/\text{W}$ |
| T_{sol} | Wave Solder Pb-Free | | | 265 | $^{\circ}\text{C}$ |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 9. DC CHARACTERISTICS, PECL V

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Table 10. DC CHARACTERISTICS, NECL $V_{CC} = 0\text{ V}$, $V_{EE} = -3.3\text{ V}$ (Note 5)

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|----------|---|-------|-------|-------|-------|-------|-------|-------|-------|-------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I_{EE} | Power Supply Current | 100 | 125 | 160 | 110 | 130 | 170 | 110 | 135 | 175 | mA |
| V_{OH} | Output HIGH Voltage (Note 6) | -1145 | -1000 | -895 | -1145 | -1000 | -895 | -1145 | -1000 | -895 | mV |
| V_{OL} | Output LOW Voltage (Note 6) | -1995 | -1780 | -1695 | -1995 | -1800 | -1695 | -1995 | -1815 | -1695 | mV |
| V_{IH} | Input HIGH Voltage (Single-Ended) LVNECL | -1225 | | -880 | -1225 | | -880 | -1225 | | -880 | mV |
| V_{IL} | Input LOW Voltage (Single-Ended) LVNECL | -1995 | | -1625 | -1995 | | -1625 | -1995 | | -1625 | mV |
| V_{BB} | | | | | | | | | | | |

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Table 11. AC CHARACTERISTICS $V_{CC} = 0\text{ V}$; $V_{EE} = -3.0\text{ V to } -3.6\text{ V}$ or $V_{CC} = 3.0\text{ V to } 3.6\text{ V}$; $V_{EE} = 0\text{ V}$ (Note 8)

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|--------------------------------------|---|-----------------------------|------------------------------|------------------------------|------------------------------|------------------------------|------------------------------|------------------------------|------------------------------|------------------------------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| f_{\max} | Maximum Frequency | | 1.2 | | | 1.2 | | | 1.2 | | GHz |
| t_{PLH} t_{PHL} | Propagation Delay IN to Q; D(0-9) = 0 IN to Q; D(0-9) = 1023 $\overline{\text{EN}}$ to Q; D(0-9) = 0 D10 to CASCADE | 1810 9500 1780 350 | 2210 11496 2277 450 | 2610 13500 2780 550 | 1960 10000 1930 380 | 2360 12258 2430 477 | 2760 14000 2930 580 | 2180 10955 2150 420 | 2580 13454 2650 520 | 2980 15955 3150 620 | ps |
| t_{RANGE} | Programmable Range {D(0-9) = HI} - {D(0-9) = LO} | 8600 | 9285 | 10000 | 9200 | 9897 | 10700 | 9900 | 10875 | 12000 | ps |
| Δt | Step Delay (Note 9) D0 High D1 High D2 High D3 High D4 High 90 D5 High 245 D6 High 530 D7 High 1060 D8 High D9 High | | | | | | | | | | |

CASCADING MULTIPLE EP196S

To increase the programmable range of the EP196, internal cascade circuitry has been included. This circuitry allows for the cascading of multiple EP196s without the need for any external gating. Furthermore, this capability requires only one more address line per added E196. Obviously, cascading multiple programmable delay chips will result in a larger programmable range; however, this increase is at the expense of a longer minimum delay.

Figure 6 illustrates the interconnect scheme for cascading two EP196s. As can be seen, this scheme can easily be

expanded for larger EP196 chains. The D10 input of the EP196 is the cascade control pin and when assert **HIGH** switches output pin **CASCADE** to **LOW** and pin **CASCADE** to **LOW**. With the interconnect scheme of Figure 6 when D10 is asserted, it signals the need for a larger programmable range than is achievable with a single device. The A11 address can be added to generate a cascade output for the next EP196. For a 2–device configuration, A11 is not required.

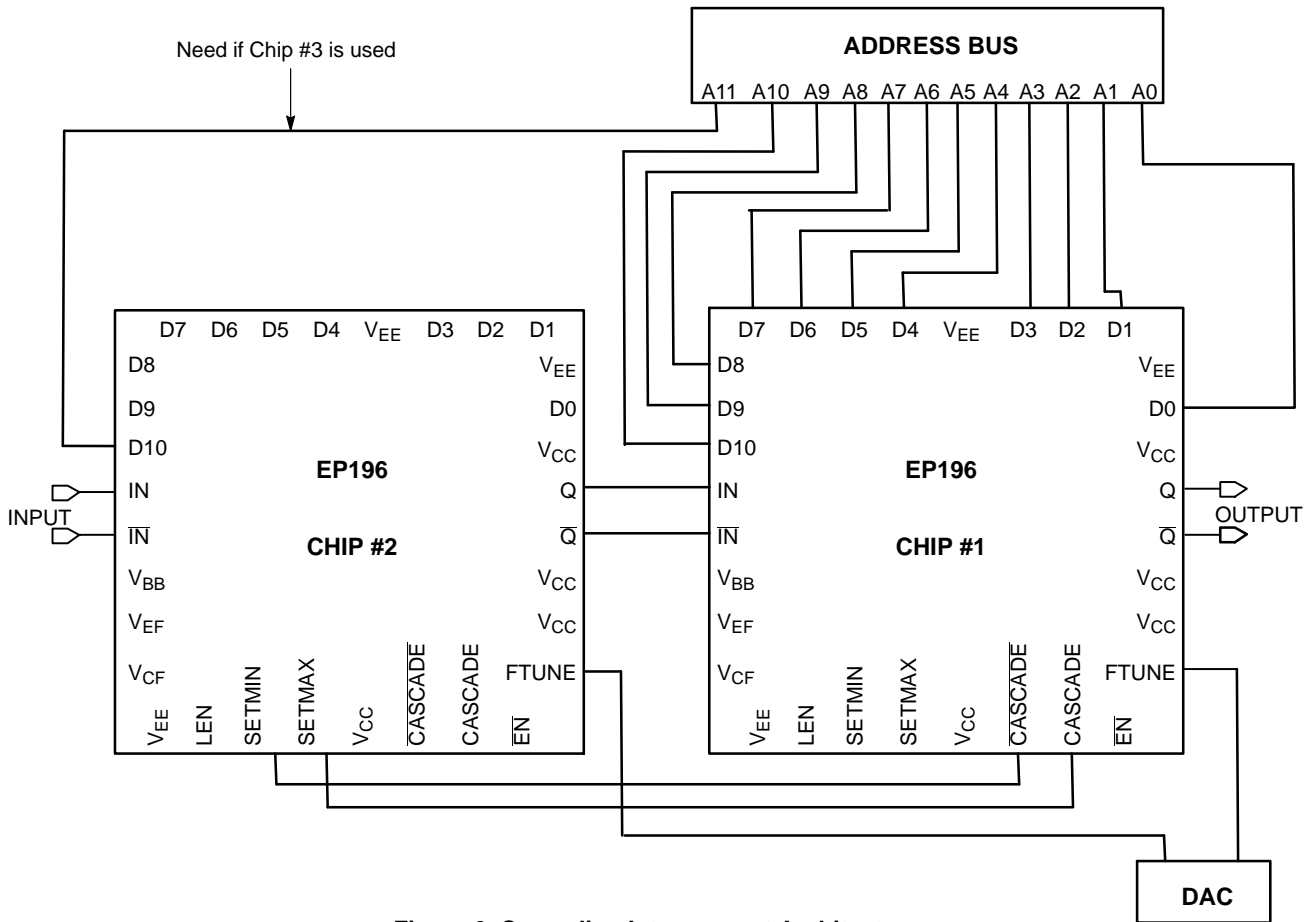


Figure 6. Cascading Interconnect Architecture

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An expansion of the latch section of the block diagram is pictured in Figure 7. Use of this diagram will simplify the explanation of how the SETMIN and SETMAX circuitry works in cascade. When D10 of chip #1 in Figure 5 is LOW, this device's cascade output will also be LOW while the CASCADE output will be HIGH. In this condition, the SETMIN pin of chip #2 will be asserted HIGH and thus all of the latches of chip #2 will be reset and the device will be set at its minimum delay.

Chip #1, on the other hand, will have both SETMIN and SETMAX deasserted so that its delay will be controlled entirely by the address bus A0–A9. If the delay needed is greater than can be achieved with 1023 gate delays (1111111111 on the A0–A9 address bus), D10 will be asserted to signal the need to cascade the delay to the next EP196 device. When D10 is asserted, the SETMIN pin of

chip #2 will be deasserted and the SETMAX pin asserted, resulting in the device delay to be the maximum delay. Table 12 shows the delay time of two EP196 chips in cascade.

To expand this cascading scheme to more devices, one simply needs to connect the D10 pin from the next chip to the address bus and CASCADE outputs to the next chip in the same manner as pictured in Figure 6. The only addition to the logic is the increase of one line to the address bus for cascade control of the second programmable delay chip.

Furthermore, to fully utilize EP196, the FTUNE pin can be used for additional delay and for finer resolution than 10 ps. As shown in Figure 5, an analog voltage input from DAC can adjust the FTUNE pin with an extra 60 ps of delay for each chip.

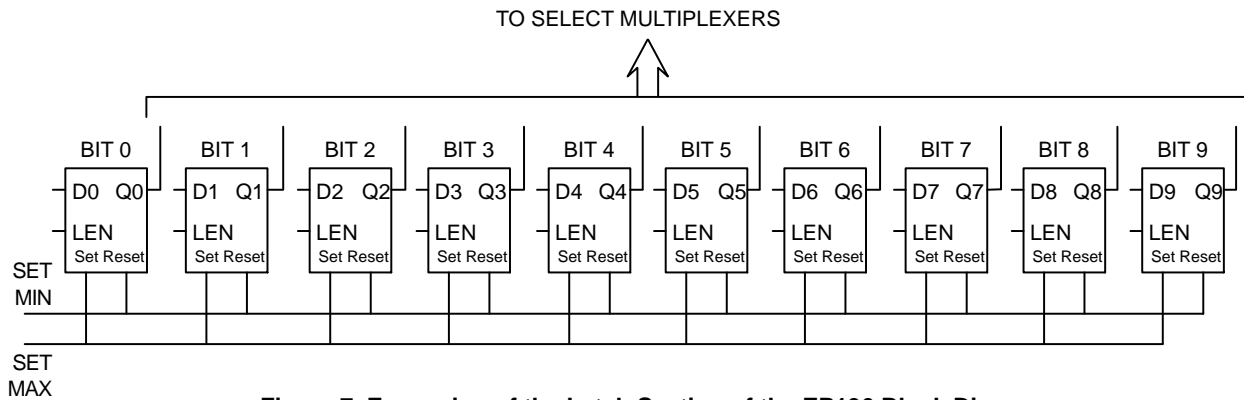


Figure 7. Expansion of the Latch Section of the EP196 Block Diagram

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Table 12. CASCADED DELAY VALUE OF TWO EP196S

| VARIABLE INPUT TO CHIP #1 AND SETMIN FOR CHIP #2 | | | | | | | | | | | | |
|--|----|----|----|----|----|----|----|----|----|----|-------------|-------------|
| INPUT FOR CHIP #1 | | | | | | | | | | | Total | |
| D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Delay Value | Delay Value |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 ps | 4400 ps |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 10 ps | 4410 ps |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 20 ps | 4420 ps |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 30 ps | 4430 ps |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 40 ps | 4440 ps |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 50 ps | 4450 ps |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 60 ps | 4460 ps |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 70 ps | 4470 ps |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 80 ps | 4480 ps |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 160 ps | 4560 ps |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 320 ps | 4720 ps |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 640 ps | 5040 ps |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1280 ps | 5680 ps |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | |

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MULTI-CHANNEL DESKEWING

The most practical application for EP196 is in multiple channel delay matching. Slight differences in impedance and cable length can create large timing skews within a high-speed system. To deskew multiple signal channels, each channel can be sent through each EP196 as shown in

Figure 8. One signal channel can be used as reference and the other EP196s can be used to adjust the delay to eliminate the timing skews. Nearly any high-speed system can be fine tuned (as small as 10 ps) to reduce the skew to extremely tight tolerances using the available FTUNE pin.

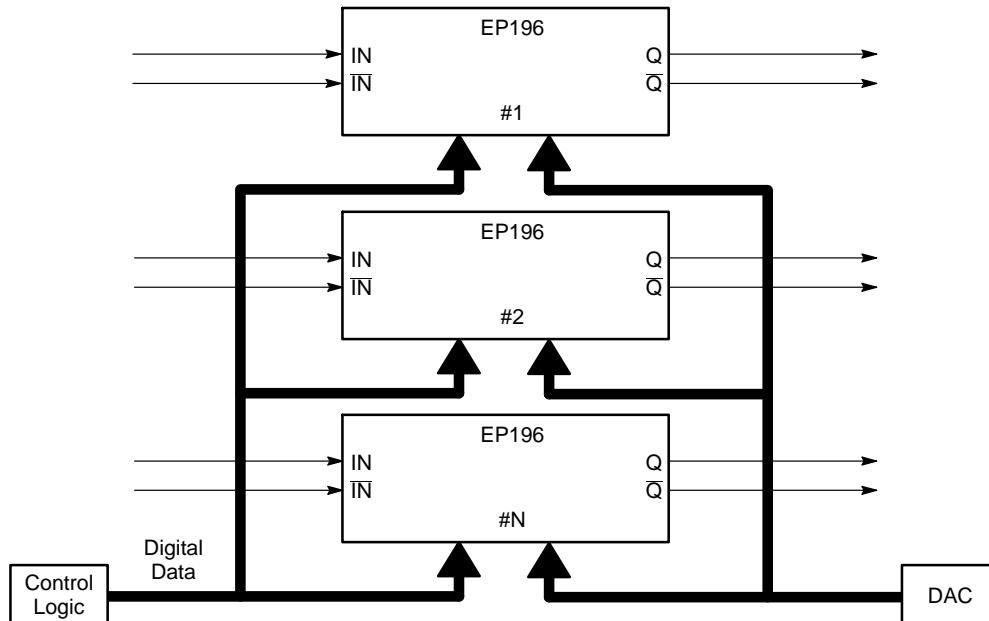


Figure 8. Multiple Channel Deskewing Diagram

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LQFP-32, 7x7
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