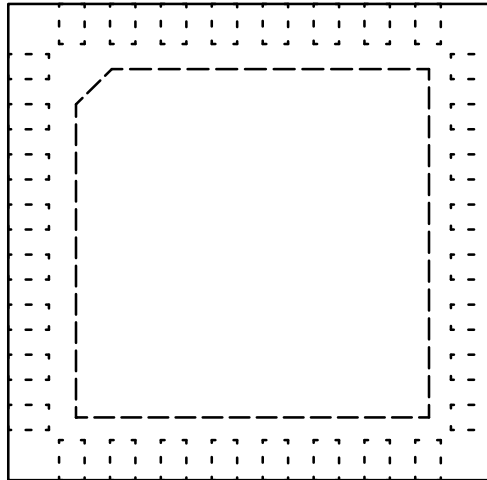


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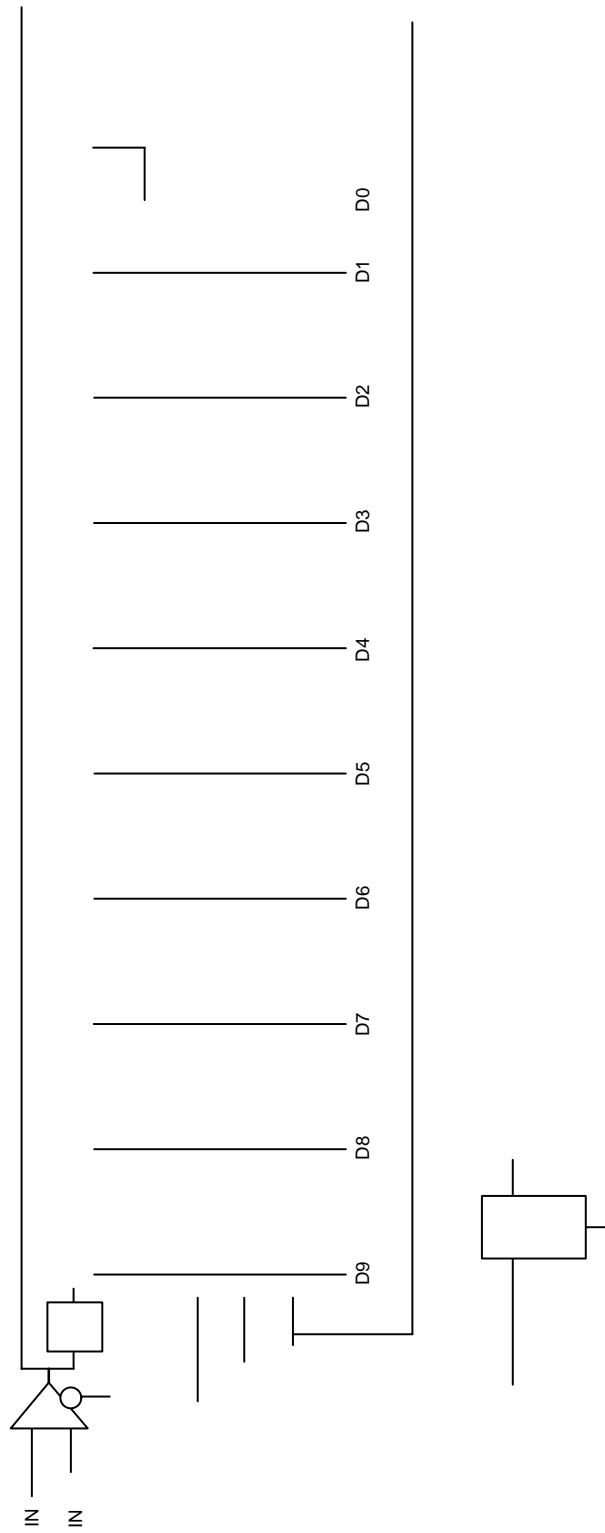


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Table 1. PIN DESCRIPTION

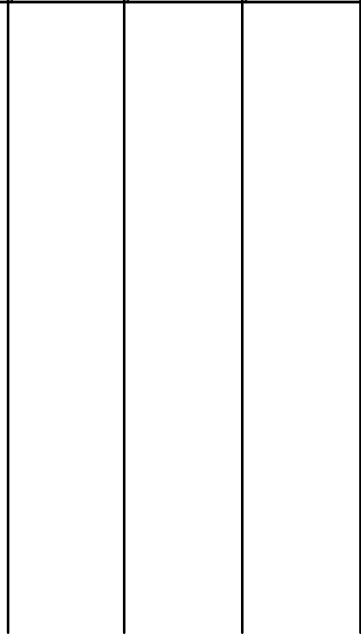
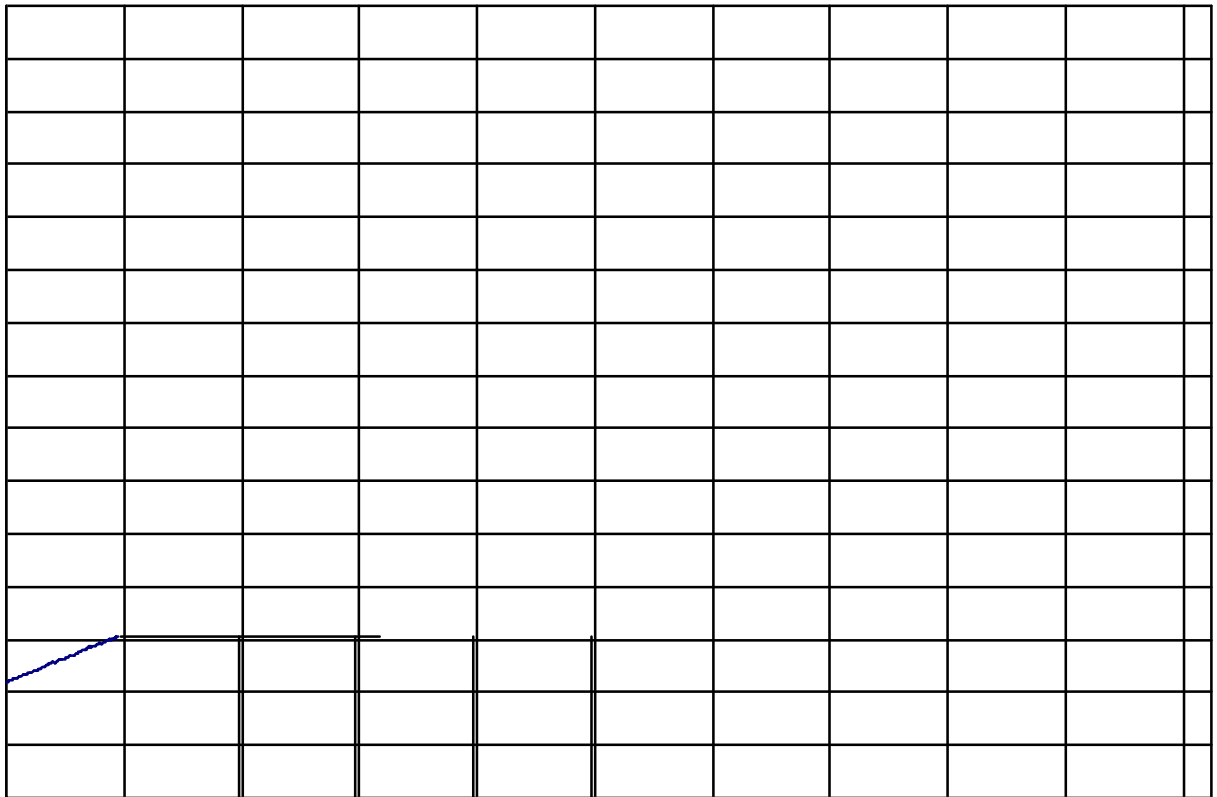
Pin	Name	I/O	Default State	Description
23, 25, 26, 27, 29, 30, 31, 32, 1, 2	D[0:9]			

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Table 9. 100EP DC CHARACTERISTICS, PECL $V_{CC} = 3.3\text{ V}$, $V_{EE} = 0\text{ V}$ (Note 7)

Symbol	Characteristic	40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Negative Power Supply Current	90	115	170	100	140	170	100	145	175	mA
V_{OH}	Output HIGH Voltage (Note 8)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
V_{OL}	Output LOW Voltage (Note 8)	1305	1480	1605	1305	1480	1605	1305	1480	1605	mV
V_{IH}	Input HIGH Voltage (Single-Ended)										mV
	LVPECL	2075		2420	2075		2420	2075		2420	
	CMOS	2000		3300	2000		3300	2000		3300	
	TTL	2000		3300	2000		3300	2000		3300	
V_{IL}	Input LOW Voltage (Single-Ended)										mV
	LVPECL	1305		1675	1305		1675	1305		1675	
	CMOS	0		800	0		800	0		800	
	TTL	0		800	0		800	0		800	
V_{BB}	ECL Output Voltage Reference	1775	1875	1975	1775	1875	1975	1775	1875	1975	mV
V_{CF}	LVTTTL Mode Input Detect Voltage	1.4	1.5	1.6	1.4	1.5	1.6	1.4	1.5	1.6	V
V_{EF}	Reference Voltage for ECL Mode Connection	1900	2020	2150	1900	2020	2150	1900	2020	2150	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 9)	1.2		3.3	1.2		3.3	1.2		3.3	V
I_{IH}	Input HIGH Current (@ V_{IH})	0		150	0		150	0		150	μA
I_{IL}	Input LOW Current (@ V_{IL})		IN, $\overline{\text{IN}}$	150							

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Table 10. 100EP DC CHARACTERISTICS, NECL $V_{CC} = 0\text{ V}$, $V_{EE} = -3.3\text{ V}$ (Note 10)

Symbol	Characteristic	40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Negative Power Supply Current (Note 11)	90	115	170	100	140	170	100	145	175	mA
V_{OH}	Output HIGH Voltage (Note 12)	-1145	-1020	-895	-1145	-1020	-895	-1145	-1020	-895	mV
V_{OL}	Output LOW Voltage (Note 12)	-1995	-1820	-1695	-1995	-1820	-1695	-1995	-1820	-1695	mV
V_{IH}	Input HIGH Voltage (Single-Ended) LVNECL	-1225		-880	-1225		-880	-1225		-880	mV
V_{IL}	Input LOW Voltage (Single-Ended) LVNECL	-1995		-1625	-1995		-1625	-1995		-1625	mV
V_{BB}	ECL Output Voltage Reference	-1525	-1425	-1325	-1525	-1425	-1325	-1525	-1425	-1325	mV
V_{EF}	Reference Voltage for ECL Mode Connection	-1400	-1280	-1250	-1400	-1280	-1250	-1400	-1280	-1250	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 13)	$V_{EE} + 1.2$		0.0	$V_{EE} + 1.2$		0.0	$V_{EE} + 1.2$		0.0	V
I_{IH}	Input HIGH Current (@ V_{IH})	0		150	0		150	0		150	μA
I_{IL}	Input LOW Current (@ V_{IL}) $I_N, \overline{I_N}$	0		150	0		150	0		150	μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

10. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.3 V to -0.3 V.

11. Required 500 lfm air flow when using +5 V power supply. For $(V_{CC} - V_{EE}) > 3.3\text{ V}$, $5\ \Omega$ to $10\ \Omega$ in line with V_{EE} required for maximum thermal protection at elevated temperatures. Recommend $V_{CC} - V_{EE}$ operation at $\leq 3.8\text{ V}$.

12. All loading with $50\ \Omega$ to $V_{CC} - 2.0\text{ V}$.

13. V_{IHCMR} min varies 1:1 with V_{EE} , V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

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Table 11. AC CHARACTERISTICS $V_{CC} = 0\text{ V}$; $V_{EE} = -3.0\text{ V}$ to -3.6 V or $V_{CC} = 3.0\text{ V}$ to 3.6 V ; $V_{EE} = 0\text{ V}$ (Note 14)

Symbol	Characteristic	40°C			25°C			85°C		Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	

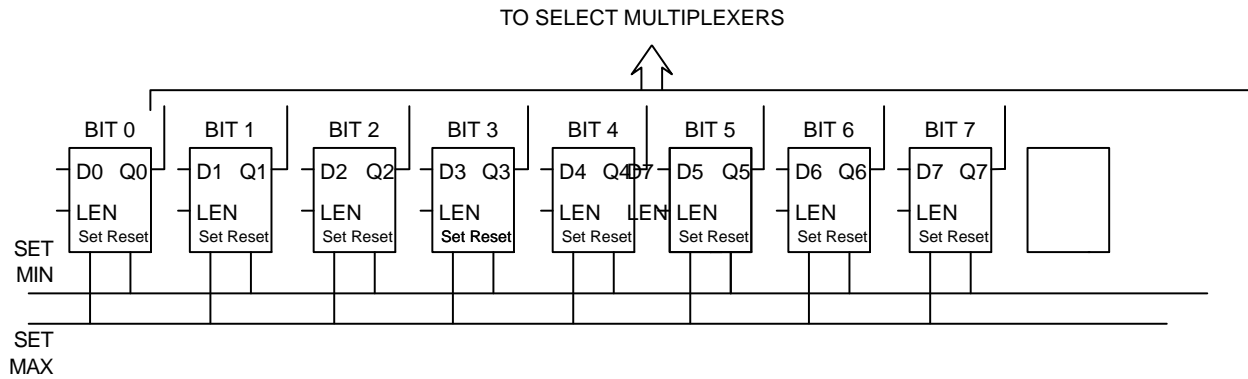
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An expansion of the latch section of the block diagram is pictured in Figure 8. Use of this diagram will simplify the explanation of how the cascade circuitry works. When D10 of chip #1 in Figure 7 is LOW this device's CASCADE output will also be low while the CASCADE output will be high. In this condition the SET MIN pin of chip #2 will be asserted HIGH and thus all of the latches of chip #2 will be reset and the device will be set at its minimum delay.

Chip #1, on the other hand, will have both SET MIN and SET MAX deasserted so that its delay will be controlled entirely by the address bus A0—A9. If the delay needed is greater than can be achieved with 1023 gate delays

(111111111 on the A0—A9 address bus) D10 will be asserted to signal the need to cascade the delay to the next EP196B device. When D10 is asserted, the SET MIN pin of chip #2 will be deasserted and SET MAX pin asserted resulting in the device delay to be the maximum delay. Table 12 shows the delay time of two EP196B chips in cascade.

To expand this cascading scheme to more devices, one simply needs to connect the D10 pin from the next chip to the address bus and CASCADE outputs to the next chip in the same manner as pictured in Figure 7. The only addition to the logic is the increase of one line to the address bus for cascade control of the second programmable delay chip.

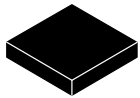


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Multi Channel Deskewing

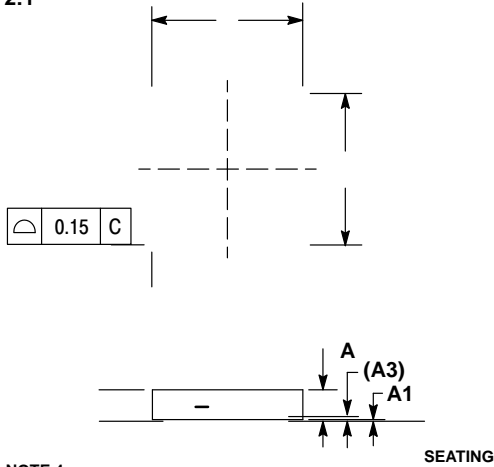
The most practical application for EP196B is in multiple channel delay matching. Slight differences in impedance and cable length can create large timing skews within a high-speed system. To deskew multiple signal channels, each channel can



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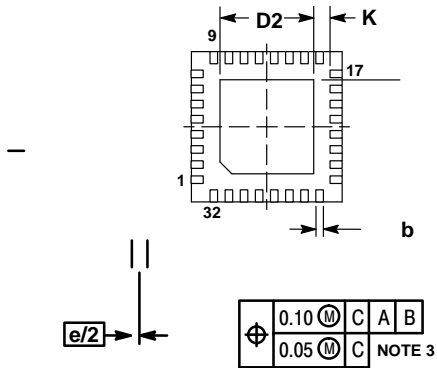
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SCALE 2:1

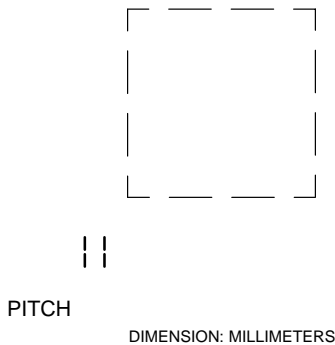


NOTE 4

	MAX
A1	0.80 1.00
A3	0.20 REF 0.05
b	0.18 0.30
D	5.00 BSC
D2	2.95 3.25
E	5.00 BSC
E2	2.95 3.25
e	0.50 BSC
K	0.20
L	0.30 0.50
L1	0.15



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