# 3.3 V/5 V ECL D Flip-Flop with Set and Reset

# MC100EP31

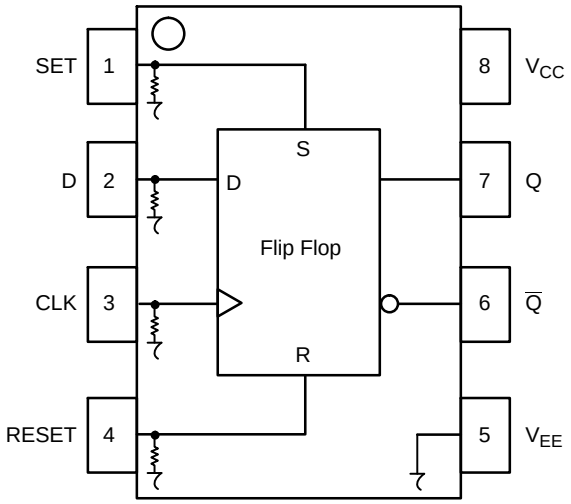
The MC100EP31 is a D flip-flop with set and reset. The device is pin and functionally equivalent to the EL31 and LVEL31 devices. With AC performance much faster than the EL31 and LVEL31 devices, the EP31 is ideal for applications requiring the fastest AC performance available. Both set and reset inputs are asynchronous, level triggered signals. Data enters the master portion of the flip-flop when CLK is low and is transferred to the slave, and thus the outputs, upon a positive transition of the CLK.

The 100 Series contains temperature compensation.

- 340 ps Typical Propagation Delay
- Maximum Frequency = > 3 GHz Typical
- PECL Mode Operating Range:
  $V_{CC}$ = 3.0 V to 5.5 V with $V_{EE}$ = 0 V
- NECL Mode Operating Range:
  $V_{CC}$ = 0 V with $V_{EE}$ = 3.0 V to 5.5 V
- Open Input Default State
- Q Output Will Default LOW with Inputs Open or at $V_{EE}$
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant



Publication Order Number:




(Top View)

| | |
|---|---|
| CLK* | ECL Clock Inputs |
| Reset* | ECL Asynchronous Reset |
| Set* | ECL Asynchronous Set |
| D* | ECL Data Input |
| Q, $\overline{Q}$ | ECL Data Outputs |
| $V_{CC}$ | Positive Supply |
| $V_{EE}$ | Negative Supply |

*Pins will default LOW when left open.

| | | | | |
|---|---|---|---|---|
| L | L | L | Z | L |
| H | L | L | Z | H |
| X | H | L | X | H |
| X | L | H | X | L |
| X | H | H | X | UNDEF |

Z = LOW to HIGH Transition

| | |
|---|---|
| Internal Input Pulldown Resistor | 75 kΩ |
| Internal Input Pullup Resistor | N/A |
| ESD Protection<br>Human Body Model<br>Machine Model<br>Charged Device Model | <br>> 4 kV<br>> 200 V<br>> 2 kV |
| Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1) | Pb-Free Pkg |
| SOIC−8 NB<br>TSSOP−8 | Level 1<br>Level 3 |
| Flammability Rating<br>Oxygen Index: 28 to 34 | <br>UL 94 V−0 @ 0.125 in |
| Transistor Count | 75 Devices |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test | |

1. For additional information, see Application Note AND8003/D.

| | | | | | |
|---|---|---|---|---|---|
| $V_{CC}$ | PECL Mode Power Supply | $V_{EE}$ = 0 V | | 6 | V |
| $V_{EE}$ | NECL Mode Power Supply | $V_{CC}$ = 0 V | | −6 | V |
| $V_I$ | PECL Mode Input Voltage<br>NECL Mode Input Voltage | $V_{EE}$ = 0 V<br>$V_{CC}$ = 0 V | $V_I \le V_{CC}$<br>V | | |

($V_{CC}$ = 0 V; $V_{EE}$ = −3.0 V to −5.5 V or $V_{CC}$ = 3.0 V to 5.5 V; $V_{EE}$ = 0 V (Note 1))

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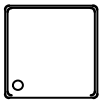
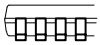
| $f_{max}$ | | | | | | | | | | | |

**TSSOP 8 3.00x3.00x0.95**
CASE 948R−02
ISSUE A

DATE 07 APR 2000





| DIM | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 2.90 | 3.10 | 0.114 | 0.122 |
| B | | | | |
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