

3.3 V/5 V ECL JK Fli -FI

MC100EP35

Description

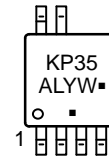
The MC100EP35 is a higher speed/low voltage version of the EL35 JK flip-flop. The J/K data enters the master portion of the flip-flop when the clock is LOW and is transferred to the slave, and thus the outputs, upon a positive transition of the clock. The reset pin is asynchronous and is activated with a logic HIGH.

The 100 Series contains temperature compensation.

Features

- 410 ps Propagation Delay
- Maximum Frequency > 3 GHz Typical
- PECL Mode Operating Range:
 - ◆ $V_{CC} = 3.0\text{ V to }5.5\text{ V}$ with $V_{EE} = 0\text{ V}$
- NECL Mode Operating Range:
 - ◆ $V_{CC} = 0\text{ V}$ with $V_{EE} = -3.0\text{ V to }-5.5\text{ V}$
- Open Input Default State
- Q Output Will Default LOW with Inputs Open or at V_{EE}
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

MARKING DIAGRAM*



- K = MC100
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

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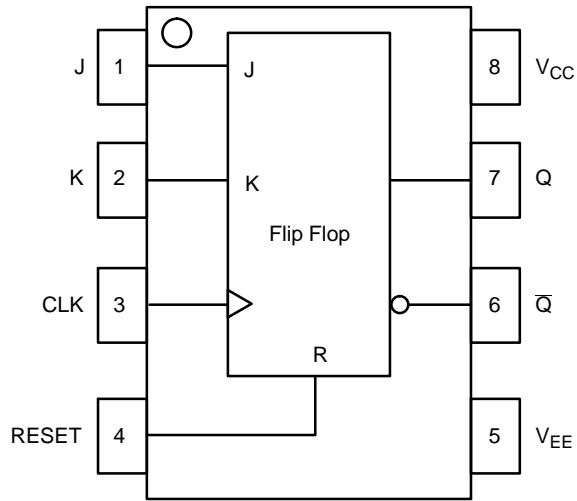


Table 1. PIN DESCRIPTION

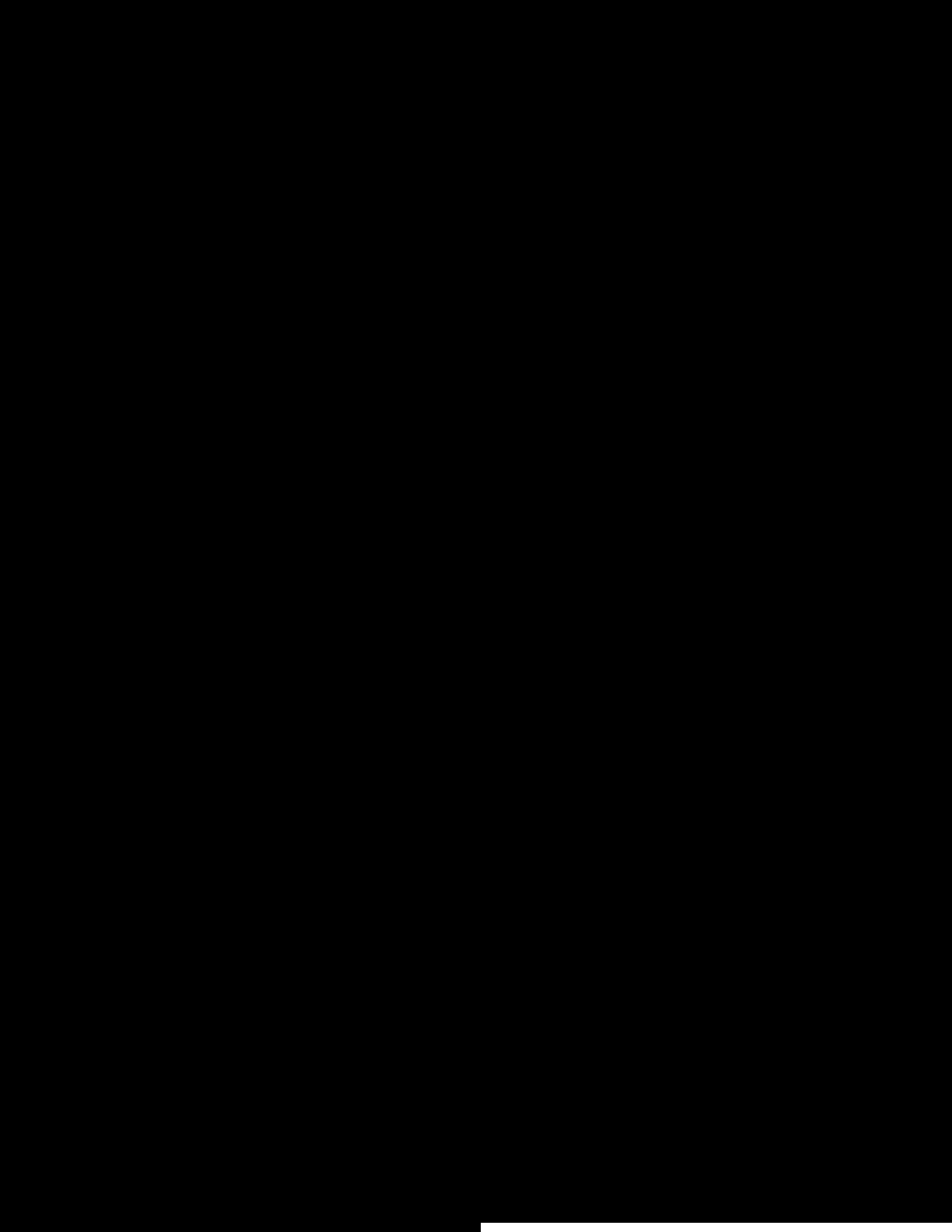
PIN	FUNCTION
CLK*	ECL Clock Inputs
J*, K*	ECL Signal Inputs

Figure 1. 8-Lead Pinout (Top View) and Logic Diagram

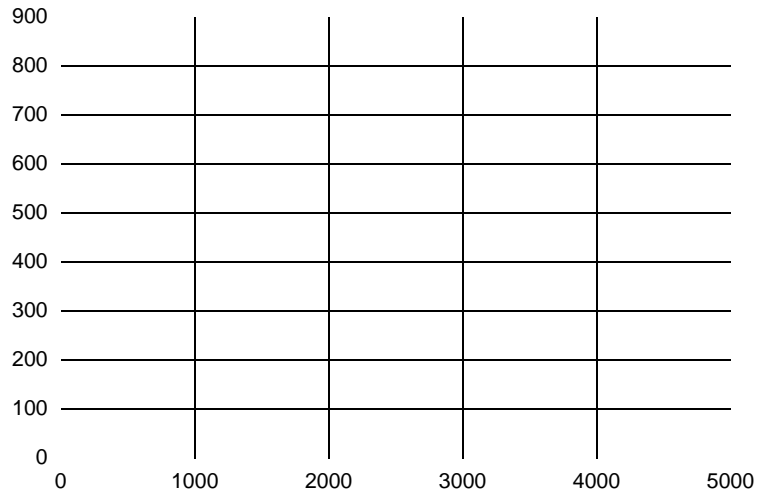
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Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	PECL Mode Power Supply	$V_{EE} = 0\text{ V}$		6	V
V_{EE}	NECL Mode Power Supply	$V_{CC} = 0\text{ V}$		-6	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	$V_{EE} = 0\text{ V}$ $V_{CC} = 0\text{ V}$	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 -6	V
I_{out}	Output Current	Continuous Surge		50 100	mA
T_A	Operating Temperature Range			-40 to +85	°C
T_{stg}	Storage Temperature Range			-65 to +150	°C



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