



MC100EP40

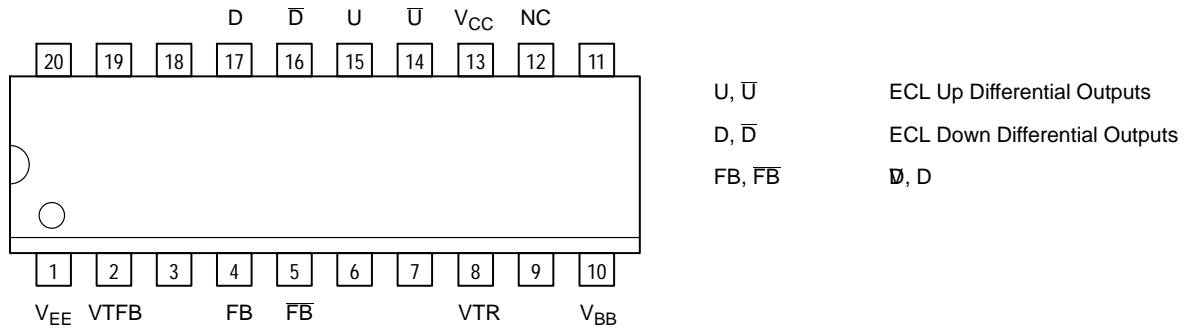


Figure 1. 20-Lead Pinout (Top View)

Figure 2. Logic Diagram

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Table 2. ATTRIBUTES

Characteristics		Value	
Internal Input Pulldown Resistor		N/A	
Internal Input Pullup Resistor		N/A	
ESD Protection	Human Body Model Machine Model Charged Device Model	> 4 kV > 100 V > 2 kV	
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)		Pb Pkg	Pb-Free Pkg
TSSOP-20		Level 1	Level 3
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
Transistor Count		699 Devices	
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test			

1. For additional information, see Application Note AND8003/D.

Table 3. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	PECL Mode Power Supply	$V_{EE} = 0\text{ V}$		6	V
V_{EE}	NECL Mode Power Supply	$V_{CC} = 0\text{ V}$		-6	V
V_I	PECL Mode Input Voltage	$V_{EE} = 0\text{ V}$	$V_I \leq V_{CC}$	6	V
	NECL Mode Input Voltage	$V_{CC} = 0\text{ V}$	$V_I \geq V_{EE}$	-6	V
I_{out}	Output Current	Continuous Surge		50	mA
				100	mA
I_{BB}	V_{BB} Sink/Source			0.5	mA
T_A	Operating Temperature Range			-40 to +85	C
T_{stg}	Storage Temperature Range			-65 to +150	C
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm	TSSOP-20	140	C/W
		500 lfpm	TSSOP-20	100	C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	TSSOP-20		

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Table 4. 100EP DC CHARACTERISTICS, PECL $V_{CC} = 3.3\text{ V}$, $V_{EE} = 0\text{ V}$ (Note 2)

Symbol	Characteristic	-40 C			25 C			85 C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	100	128	160	100	130	160	110	140	170	mA
V_{OH}	Output HIGH Voltage (Note 3)	2225	2350	2475	2275	2400	2525	2300	2425	2550	mV

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Table 6. 100EP DC CHARACTERISTICS, NECL $V_{CC} = 0\text{ V}$; $V_{EE} = -5.5\text{ V}$ to -3.0 V (Note 9)

Symbol	Characteristic	-40 C			25 C			85 C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current (Note 10)	100	128	160	100	130	160	110	140	170	mA
V_{OH}	Output HIGH Voltage (Note 11)	-1075	-950	-825	-1025	-900	-775	-1000	-875	-750	mV
V_{OL}	Output LOW Voltage (Note 11) U, U, B, B PLD	-1525 -1995	-1400 -1820	-1275 -1695	-1500 -1995	-1375 -1820	-1250 -1695	-1475 -1995	-1350 -1820	-1225 -1695	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	-1225		-880	-1225		-880	-1225		-880	mV
V_{IL}	Input LOW Voltage (Single-Ended)	-1995		-1625	-1995		-1625	-1995		-1625	mV
V_{BB}	Output Voltage Reference	-1525	-1425	-1325	-1525	-1425	-1325	-1525	-1425	-1325	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 12)	$V_{EE} + 2.0$		0.0	$V_{EE} + 2.0$		0.0	$V_{EE} + 2.0$		0.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	-150			-150			-150			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm.

9. Input and output parameters vary 1:1 with V_{CC} .

10. For $(V_{CC} - V_{EE}) > 3.3\text{ V}$, $5\ \Omega$ to $10\ \Omega$ in line with V_{EE} required for maximum thermal protection at elevated temperatures. Recommend $V_{CC}-V_{EE}$ operation at $\leq 3.3\text{ V}$.

11. All loading with $50\ \Omega$ to $V_{CC} - 2.0\text{ V}$.

12. V_{IHCMR} min varies 1:1 with V_{EE} , V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 7. AC CHARACTERISTICS $V_{CC} = 0\text{ V}$; $V_{EE} = -3.0\text{ V}$ to -5.5 V or $V_{CC} = 3.0\text{ V}$ to 5.5 V ; $V_{EE} = 0\text{ V}$ (Note 13)

Symbol	Characteristic	-40 C			25 C			85 C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Frequency (Figure 3)		> 2			> 2			> 2		GHz
t_{PLH} , t_{PHL}	Propagation Delay to Output Differential FB to D/U R to D/U	400	525	700	410	550	750	450	575	775	ps
t_{JITTER}	Random Clock Jitter (Figure 3)		0.2	< 1		0.2	< 1		0.2	< 1	ps
V_{PP}	Input Voltage Swing (Differential Configuration)	150	800	1200	150	800	1200	150	800	1200	mV
t_r , t_f	Output Rise/Fall Times Q, \bar{Q} (20% - 80%)	60	85	130	60	110	150	80	120	160	ps

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm.

13. Measured using a 750 mV source, 50% duty cycle clock source. All loading with $50\ \Omega$ to $V_{CC} - 2.0\text{ V}$.

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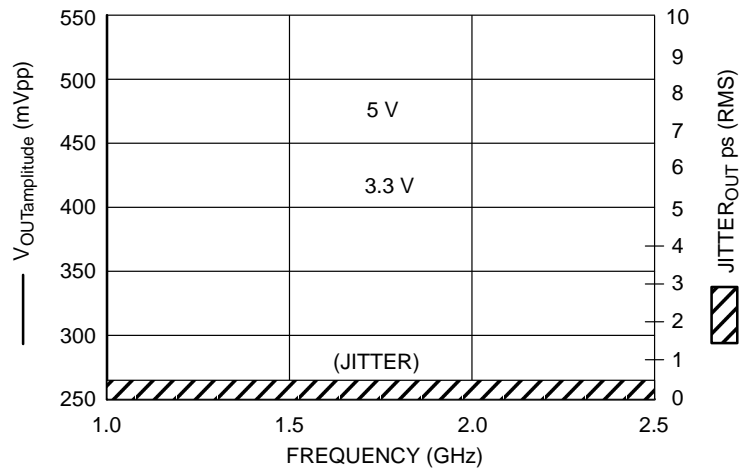


Figure 3. $F_{max}/Jitter @ 25^{\circ}C$

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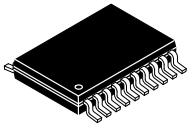
Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPiCE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

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PACKAGE DIMENSIONS



CALE 2:1

TSSOP-20 WB
CASE 948E
ISSUE D

DATE 17 FEB 2016

NOTES:

DIM	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A		6.60		0.260
B	4.30	4.50	0.169	0.177
C		1.20		0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

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