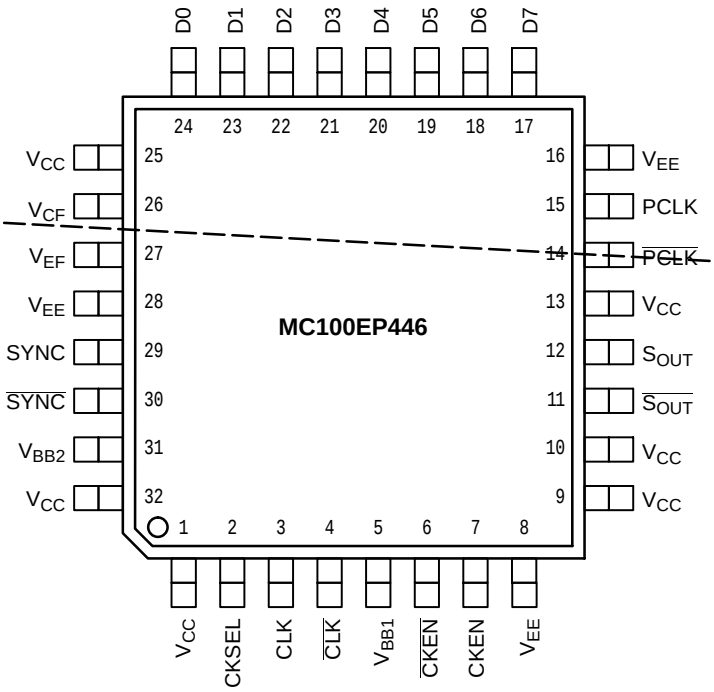


Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. LQFP−32 Pinout (Top View)

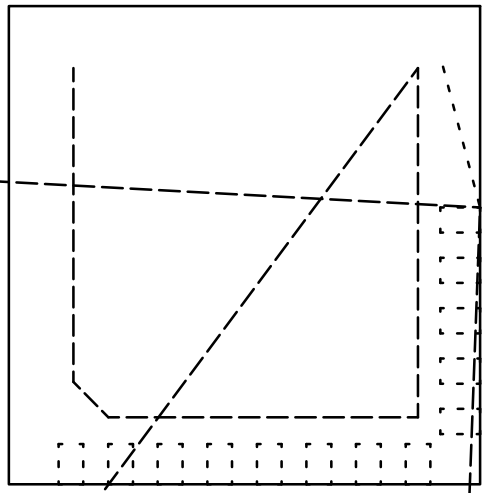
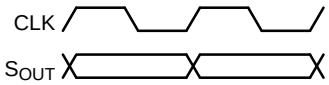
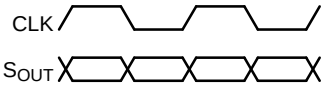


Figure 2. QFN−32 Pinout (Top View)

Table 2. TRUTH TABLE

Pin	Function	
	HIGH	LOW
CKSEL	S_{OUT}: PCLK = 8:1 CLK: S_{OUT} = 1:1 	S_{OUT}: PCLK = 8:1 CLK: S_{OUT} = 1:2 
CKEN	Synchronously Disables Normal Parallel to Serial Conversion	Synchronously Enables Normal Parallel to Serial Conversion
SYNC	Asynchronously Resets Internal Flip−Flops*	Synchronous Enable

*The rising edge of SYNC will asynchronously reset the internal circuitry. The falling edge of the SYNC followed by the falling edge of CLK initiates the conversion process synchronously on the next rising edge of CLK.

Table 3. INPUT VOLTAGE LEVEL SELECTION TABLE

Input Function	Connect To V_{CF} Pin
ECL Mode	V_{EF} Pin
CMOS Mode	No Connect
TTL Mode*	1.5 V ± 100 mV

*For TTL Mode, if no external voltage can be provided, the reference voltage can be provided by connecting the appropriate resistor between V_{CF} and V_{EE} pins.

Table 4. DATA INPUT OPERATING VOLTAGE TABLE

Power Supply (V_{CC},V_{EE})	Data Inputs (D [0:7])			
	CMOS	TTL	PECL	NECL
PECL	√	√	√	N/A
NECL	N/A	N/A	N/A	√

Power Supply	Resistor Value 10% (Tolerance)
3.3 V	1.5 kΩ
5.0 V	500 Ω

Table 5. ATTRIBUTES

Characteristics	Value
Internal Input Pulldown Resistor	75 kΩ
Internal Input Pullup Resistor	

Table 7. 100EP DC CHARACTERISTICS, PECL V_{CC} = 3.3 V, V_{EE} = 0 V (Note 2)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	90	110	130	90	110	130	95	115	135	mA
V_{OH}	Output HIGH Voltage (Note 3)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
V_{OL}	Output LOW Voltage (Note 3)	1305	1480	1605	1305	1480	1605	1305	1480	1605	mV
V_{IH}	Input HIGH Voltage (Single−Ended) CMOS PECL TTL	 2000 2075 2000		 3300 3300 3300	 2000 2075 2000		 3300 3300 3300	 2000 2075 2000		 3300 3300 3300	mV
V_{IL}	Input LOW Voltage (Single−Ended) CMOS PECL TTL	 0 1305 0		 800 1675 800	 0 1305 0		 800 1675 800	 0 1305 0		 800 1675 800	mV
V_{BB}	Output Voltage Reference	1775	1875	1975	1775	1875	1975	1775	1875	1975	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 4)	2.0		3.3	2.0		3.3	2.0		3.3	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

Table 8. 100EP DC CHARACTERISTICS, PECL V_{CC} = 5.0 V, V_{EE} = 0 V (Note 5)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	90	110	130	90	110	130	95	115	135	mA
V_{OH}	Output HIGH Voltage (Note 6)	3855	3980	4105	3855	3980	4105	3855	3980	4105	mV
V_{OL}	Output LOW Voltage (Note 6)	3005	3180	3305	3005	3180	3305	3005	3180	3305	mV
V_{IH}	Input HIGH Voltage (Single										

Table 10. AC CHARACTERISTICS V_{CC} = 0 V; V_{EE} = −3.0 V to −5.5 V or V_{CC} = 3.0 V to 5.5 V; V_{EE} = 0 V (Note 11)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Frequency (Figure 15)										
	CKSEL High	3.2	3.4		3.2	3.4		3.2	3.4		GHz
	CKSEL Low	1.6	1.7		1.6	1.7		1.6	1.7		
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential CKSEL = 0 CLK TO S_{OUT},										

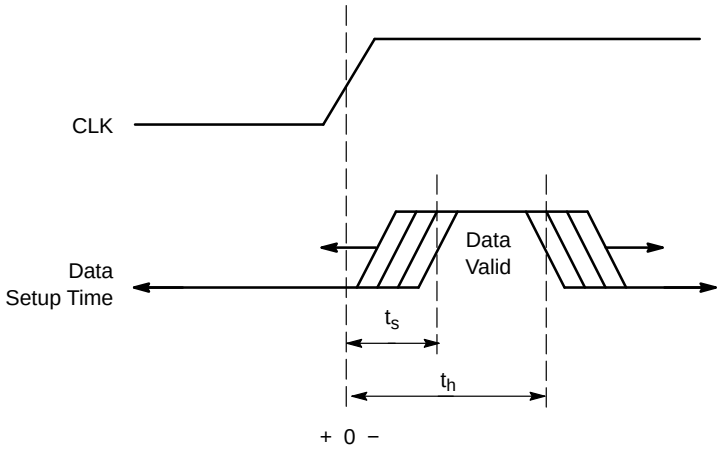


Figure 4. Setup and Hold Time for Data

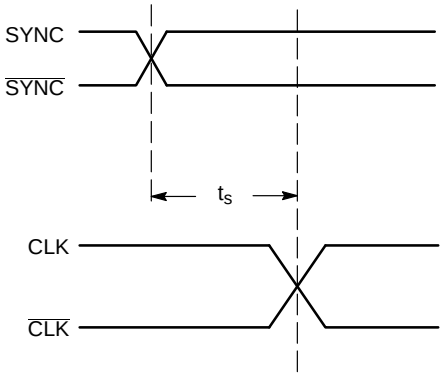


Figure 5. Setup Time for SYNC

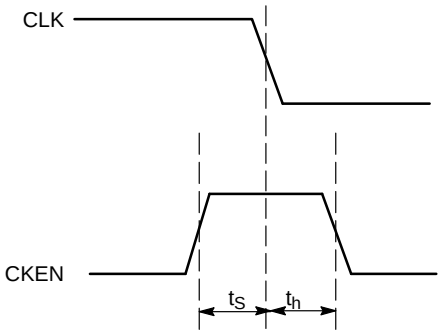


Figure 6. Setup and Hold Time for CKEN

Similarly, for CKSEL HIGH operation, the time from when the parallel data is latched ① to when the data is seen on the S_{OUT} ② is on the rising edge of the 14th clock cycle plus internal propagation delay (Figure 8). Furthermore, the PCLK switches on the rising edge of CLK.

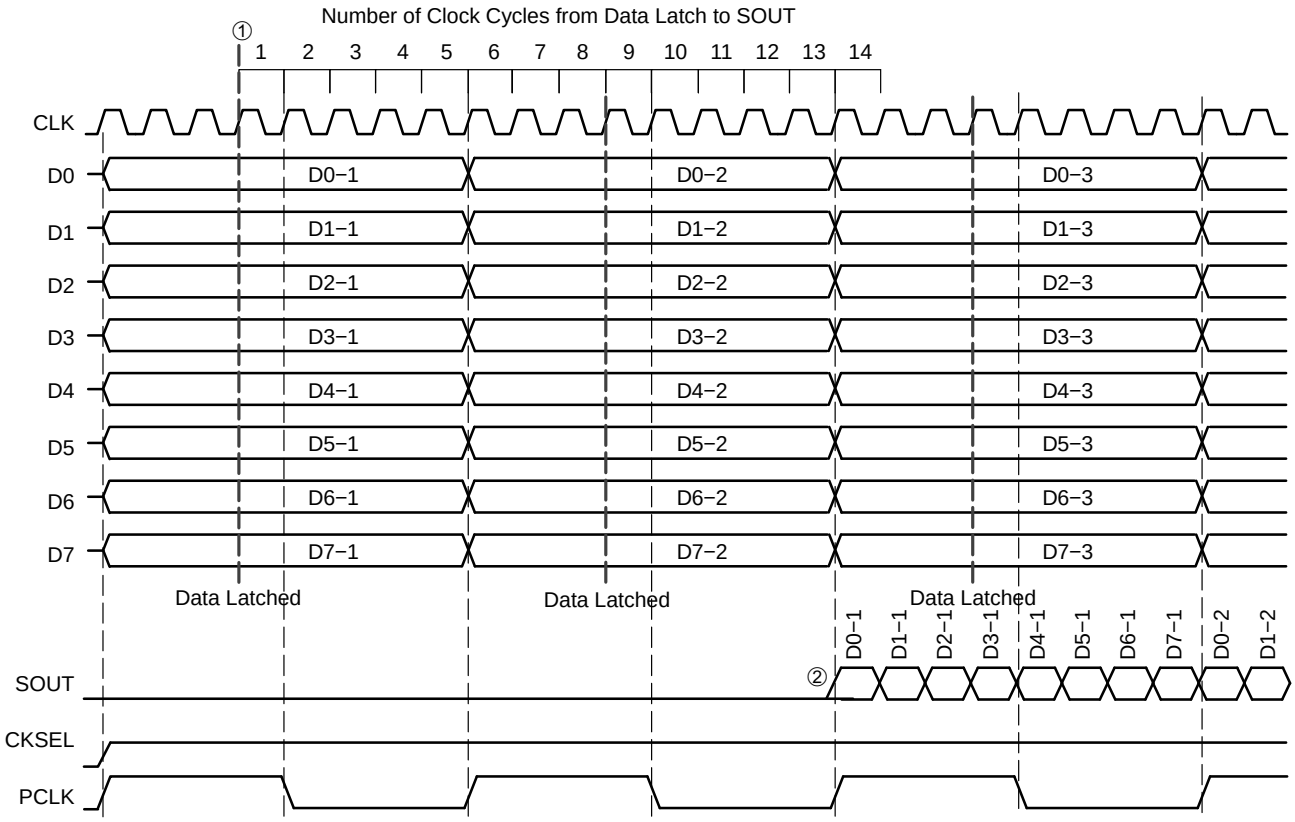


Figure 8. Timing Diagram 1:8 Parallel to Serial Conversion with CKSEL HIGH

The device also features a differential SYNC input (Pins 29 and 30), which asynchronously reset all internal flip–flops and clock circuitry on the rising edge of SYNC. The release of SYNC is a synchronous process, which ensures that no runt serial data bits are generated. The falling edge of the SYNC followed by a falling edge of CLK initiates the start of the conversion process on the next rising edge of CLK (Figures 9 and 10). As shown in the figures below, the device will start to latch the parallel

The differential synchronous CKEN inputs (Pins 6 and 7), disable the internal clock circuitry. The synchronous CKEN will suspend all of the device activities and prevent runt pulses from being generated. The rising edge of CKEN followed by the falling edge of CLK will suspend all activities. The falling edge of CKEN followed by the falling edge of CLK will resume all activities (Figure 13).

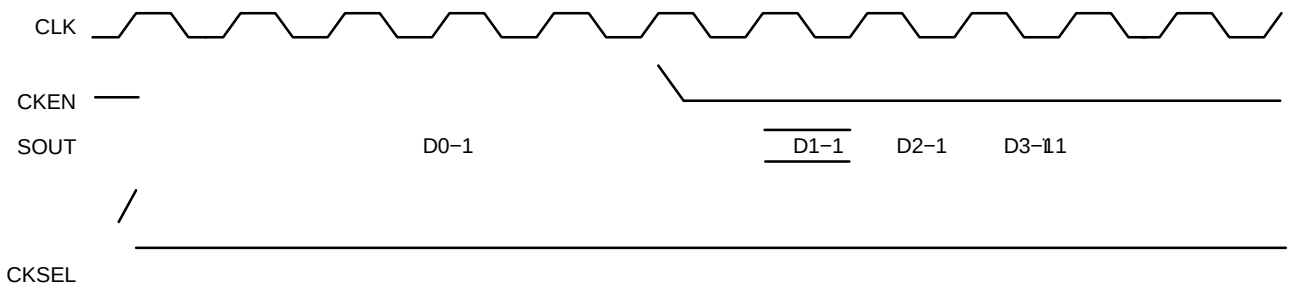


Figure 13. Timing Diagram with CKEN with CKSEL HIGH

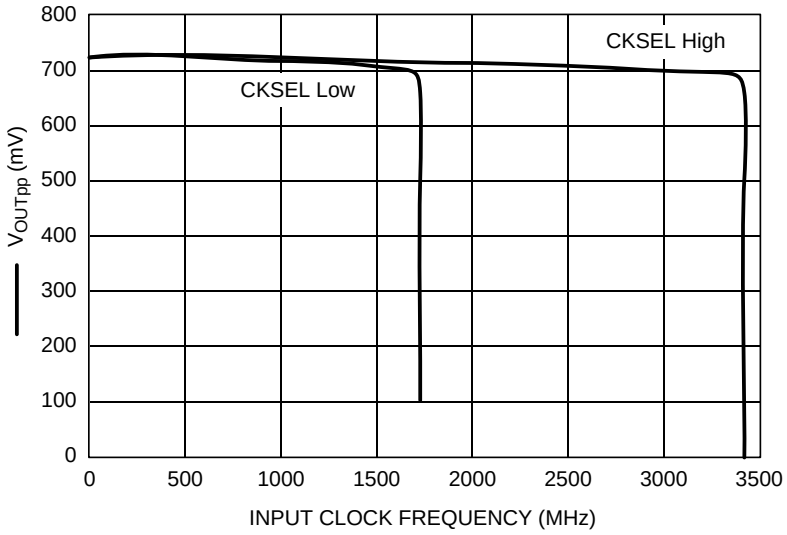


Figure 15. Typical V_{OUTPP} versus Input Clock Frequency, 25°C

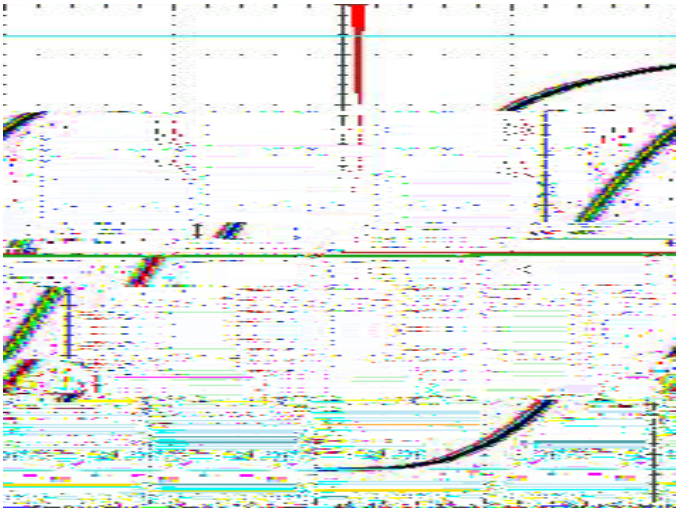


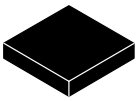
Figure 16. SOUT System Jitter Measurement
(Condition: 3.4 GHz input frequency, CKSEL HIGH, BEOFE32 bit pattern on SOUT

**Figure 17. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020/D − Termination of ECL Logic Devices.)**

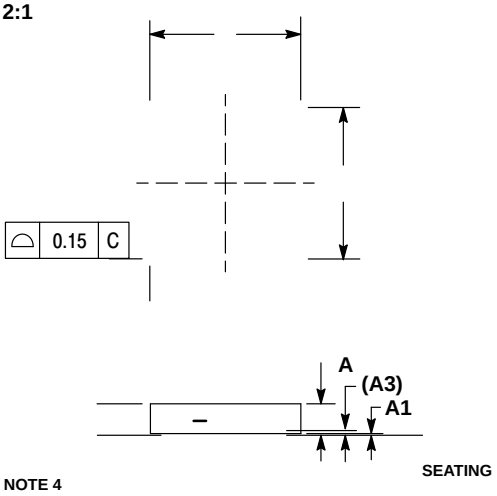
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

QFN32 5x5, 0.5P
CASE 488AM
ISSUE A

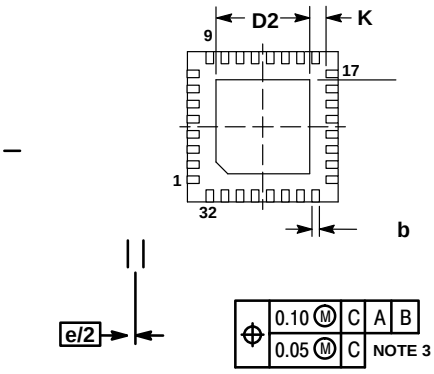
DATE 23 OCT 2013



SCALE 2:1



	MIN	MAX
A	0.80	1.00
A1	---	0.05
A3	0.20 REF	
b	0.18	0.30
D	5.00 BSC	
D2	2.95	3.25
E	5.00 BSC	
E2	2.95	3.25
e	0.50 BSC	
K	0.20	---
L	0.30	0.50
L1	---	0.15



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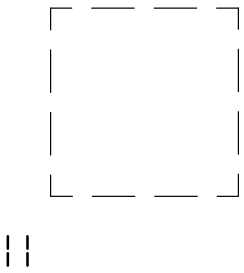
XXXXXXXX
AWLYYWW▪
▪Free indicator, “G” or

RECOMMENDED



PITCH

DIMENSION: MILLIMETERS

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LQFP−32, 7x7
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