# onsemi

## 2.5 V/3.3 V Any Level Positive Input to -3.3 V/-5.5 V NECL Output Translator MC100EP91

#### Description

The MC100EP91 is a triple any level positive input to NECL output translator. The device accepts LVPECL, LVTTL, LVCMOS, HSTL, CML or LVDS signals, and translates them to differential NECL output signals (3.0 V/ 5.5 V).

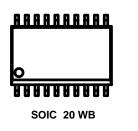
To accomplish the level translation the EP91 requires three power rails. The V<sub>CC</sub> pins should be connected to the positive power supply, and the V<sub>EE</sub> pin should be connected to the negative power supply. The GND pins are connected to the system ground plane. Both V<sub>EE</sub> and V<sub>CC</sub> should be bypassed to ground via 0.01  $\mu$ F capacitors.

Under open input conditions, the  $\overline{D}$  input will be biased at V<sub>CC</sub>/2 and the D input will be pulled to GND. These conditions will force the Q outputs to a low state, and Q outputs to a high state, which will ensure stability.

The V<sub>BB</sub> pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V<sub>BB</sub> as a switching reference voltage. V<sub>BB</sub> may also rebias AC coupled inputs. When used, decouple V<sub>BB</sub> and V<sub>CC</sub> via a 0.01  $\mu$ F capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V<sub>BB</sub> should be left open.

#### Features

Maximum Input Clock FreqDa - 1.9842.381 10 1.24 If Qq 1 0 0 1 515.56 7



QFN 24

(Note: Microdot may be in either location)

#### **ORDERING INFORMATION**

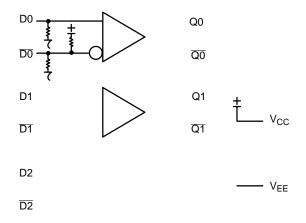
Device	Package	Shipping <sup>†</sup>			
MC100EP91MNG	QFN-24 (Pb-Free)	92 Units / Tube			

7	DISCONTINUED	(Note 1) 3/1811)13/11 C	128 I_ 79/R 06 I_1	.9842.381	10 '	1.2
-	MC100EP91DWG	SOIC-20 WB	38 Units / Tube			
		(Pb-Free)				
	MC100EP91DWR2G	SOIC-20 WB	1000 Tape & Reel			

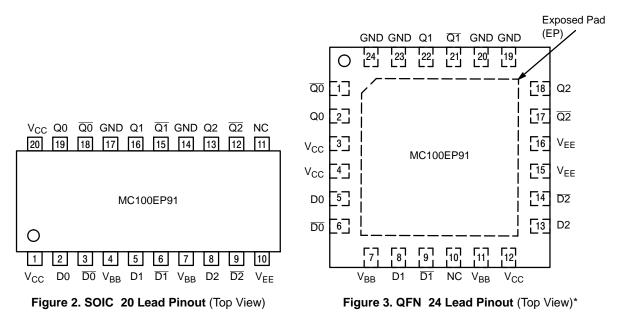
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, <u>BRD8011/D</u>.

(Pb-Free)

1. **DISCONTINUED:** This device is not recommended for new design. Please contact your **onsemi** representative for information. The most current information on this device may be available on <u>www.onsemi.com</u>.







\*All V<sub>CC</sub>, V<sub>EE</sub> and GND pins must be externally connected to a power supply and the underside exposed pad must be attached to an adequate heat–sinking conduit to guarantee proper operation.

#### Table 2. ATTRIBUTES

Characteristics	Value
Internal Input Pulldown Resistor (R1)	75 kΩ
Internal Input Pullup Resistor (R2)	75 kΩ
ESD Protection Human Body Model Machine Model Charged Device Model	> 2 kV > 150 V > 2 kV
Moisture Sensitivity (Note 1)	Pb-Free Pkg
SOIC-20 WB QFN-24	Level 3 Level 1
Flammability Rating Oxygen Index: 28 to 34	UL 94 V–0 @ 0.125 in
Transistor Count	446 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	·

#### Table 3. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V <sub>CC</sub>	Positive Power Supply	GND = 0 V		3.8 to 0	V
$V_{EE}$	Negative Power Supply	GND = 0 V		-6	V
VI	Positive Input Voltage	GND = 0 V	V <sub>I</sub> V <sub>CC</sub>	3.8 to 0	V
V <sub>OP</sub>	Operating Voltage	GND = 0 V	$V_{CC} - V_{EE}$	9.8	V
I <sub>out</sub>	Output Current	Continuous Surge		50 100	mA
I <sub>BB</sub>	PECL V <sub>BB</sub> Sink/Source			0.5	mA
T <sub>A</sub>	Operating Temperature Range			-40 to +85	С
T <sub>stg</sub>	Storage Temperature Range			-65 to +150	С
$\theta_{JA}$	Thermal Resistance (Junction-to-Ambient) JESD 51–3 (1S-Single Layer Test Board)	0 lfpm 500 lfpm	SOIC-20 WB SOIC-20 WB	90 60	C/W
$\theta_{JA}$	Thermal Resistance (Junction-to-Ambient) JESD 51–6 (2S2P Multilayer Test Board) with Filled Thermal Vias	0 lfpm 500 lfpm	QFN-24 QFN-24	37 32	C/W
$\theta_{\text{JC}}$	Thermal Resistance (Junction-to-Case)	Standard Board	SOIC-20 WB QFN-24	30 to 35 11	C/W
T <sub>sol</sub>	Wave Solder (Pb-Free)			225	С

Stresses

		40 C	25 C	85 C		l
Symbol	Characteristic	Min			Unit	

			40 C			25 C			85 C			
Symbol	Characteristic		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
V <sub>OUTPP</sub>	Output Voltage Amplitude (Figure 4) (Note 1)	f <sub>in</sub> 1.0 GHz f <sub>in</sub> 1.5 GHz f <sub>in</sub> 2.0 GHz	575 525 300	800 750 600		600 525 250	800 750 550		550 400 150	800 750 500		mV
t <sub>PLH</sub> t <sub>PHL0</sub>	Propagation Delay D to Q	Differential Single-Ended	375 300	500 450	600 650	375 300	500 450	600 675	400 300	550 500	650 750	ps
t <sub>SKEW</sub>	Pulse Skew (Note 2) Output-to-Output (Note 3) Part-to-Part (Diff) (Note 3)			15 25 50	75 95 125		15 30 50	75 105 125		15 30 70	80 105 150	ps
t <sub>JITTER</sub>	RMS Random Clock Jitter (Note 4) Peak-to-Peak Data Dependant Jitter (Note 5)	$f_{in} = 2.0 \text{ GHz}$ $f_{in} = 2.0 \text{ Gb/s}$		0.5 20	2.0		0.5 20	2.0		0.5 20	2.0	ps
V <sub>INPP</sub>	Input Voltage Swing (Differential Conf (Note 6)	iguration)	200	800	1200	200	800	1200	200	800	1200	mV
t <sub>r</sub> , t <sub>f</sub>	Output Rise/Fall Times @ 50 MHz (20 Q, Q	0%–80%)	75	150	250	75	150	250	75	150	275	ps

Table 7. AC CHARACTERISTICS ( $V_{CC} = 2.375 \text{ V}$  to 3.8 V;  $V_{EE} = -3.0 \text{ V}$  to -5.5 V; GND = 0 V)

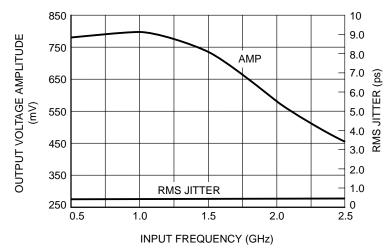
NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

1. Measured using a 750 mV source, 50% duty cycle clock source. All loading with 50 Ω to GND – 2.0 V. Input edge rates 150 ps (20% – 80%).

Pulse Skew = |t<sub>PLH</sub> - t<sub>PHL</sub>|
Skews are valid across specified voltage range, part-to-part skew is for a given temperature.

RMS Jitter with 50% Duty Cycle Input Clock Signal.
Peak-to-Peak Jitter with input NRZ PRBS 2<sup>31-1</sup> at 2.0 Gb/s.

6. Input voltage swing is a Single-Ended measurement operating in differential mode. The device has a DC gain of 50.





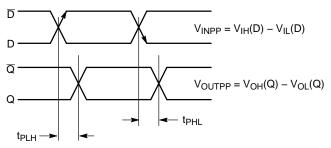


Figure 5. AC Reference Measurement

#### **Application Information**

All MC100EP91 inputs can accept LVPECL, LVTTL, LVCMOS, HSTL, CML, or LVDS signal levels. The limitations for differential input signal (LVDS, HSTL, LVPECL, or CML) are the minimum input swing of 150 mV and the maximum input swing of 3.0 V. Within these conditions, the input voltage can range from V  $_{CC}$  to GND.

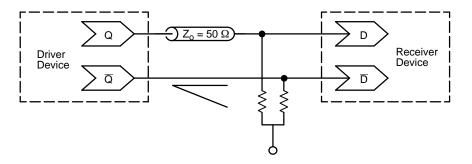
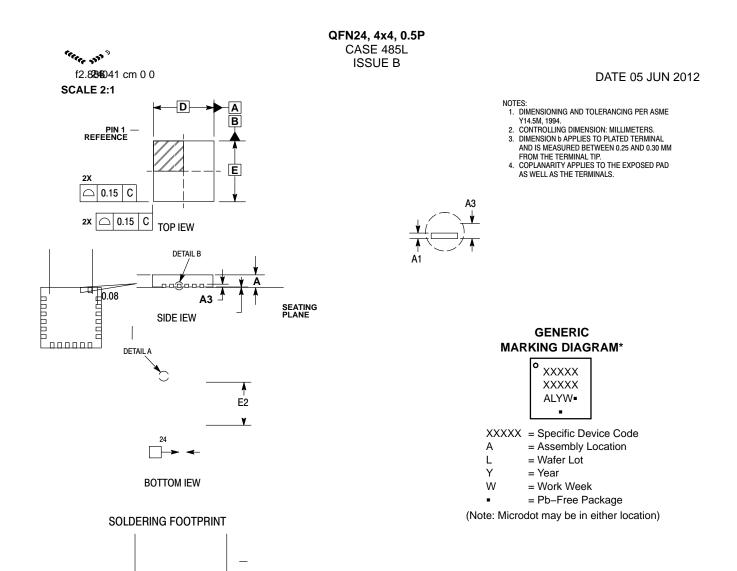


Figure 12. Typical Termination for Output Driver and Device Evaluation (See Application Note <u>AND8020/D</u> Termination of ECL Logic Devices)



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DIMENSIONS: MILLIMETERS

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