3.3V Differential LVPECL/LVDS/CML to LVTTL/LVCMOS Translator

MC100EPT21

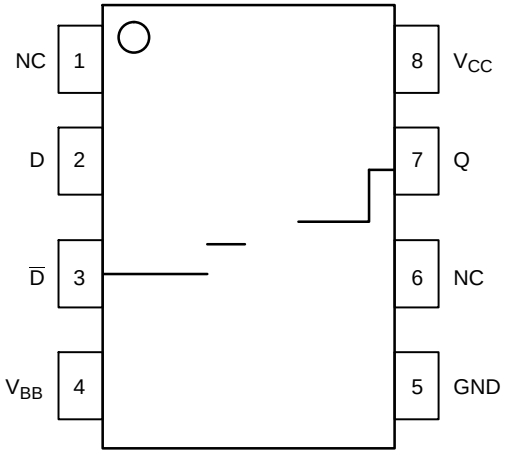
The MC100EPT21 is a Differential LVPECL/LVDS/CML to LVTTL/LVCMOS translator. Because LVPECL (Positive ECL), LVDS, and positive CML input levels and LVTTL/LVCMOS output levels are used, only +3.3 V and ground are required. The small outline 8 lead SOIC package makes the EPT21 ideal for applications which require the translation of a clock or data signal.

The V_{BB} output allows this EPT21 to be cap coupled in either single ended or differential input mode. When single ended cap coupled, V_{BB} output is tied to the $\overline{D}$ input and D is driven for a non inverting buffer, or V_{BB} output is tied to the D input and $\overline{D}$ is driven for an inverting buffer. When cap coupled differentially, V_{BB} output is connected through a resistor to each input pin. If used, the V_{BB} pin should be bypassed to V_{CC} via a 0.01 μF capacitor. For additional information see AND8020/D. For a single ended direct connection use an external voltage reference source such as a resistor divider. Do not use V_{BB} for a single ended direct connection or port to another device.

KA21
ALYW▪
▪

A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
M = Date Code
▪ = Pb−Free Package

- 1.4 ns Typical Propagation Delay
- Maximum Frequency > 275 MHz Typical
- LVPECL/LVDS/CML Inputs, LVTTL/LVCMOS Outputs
- 24 mA TTL outputs
- Operating Range: V_{CC} = 3.0 V to 3.6 V with GND = 0 V
- The 100 Series Contains Temperature Compensation
- V_{BB} Output
- These Devices are Pb Free and are RoHS Compliant

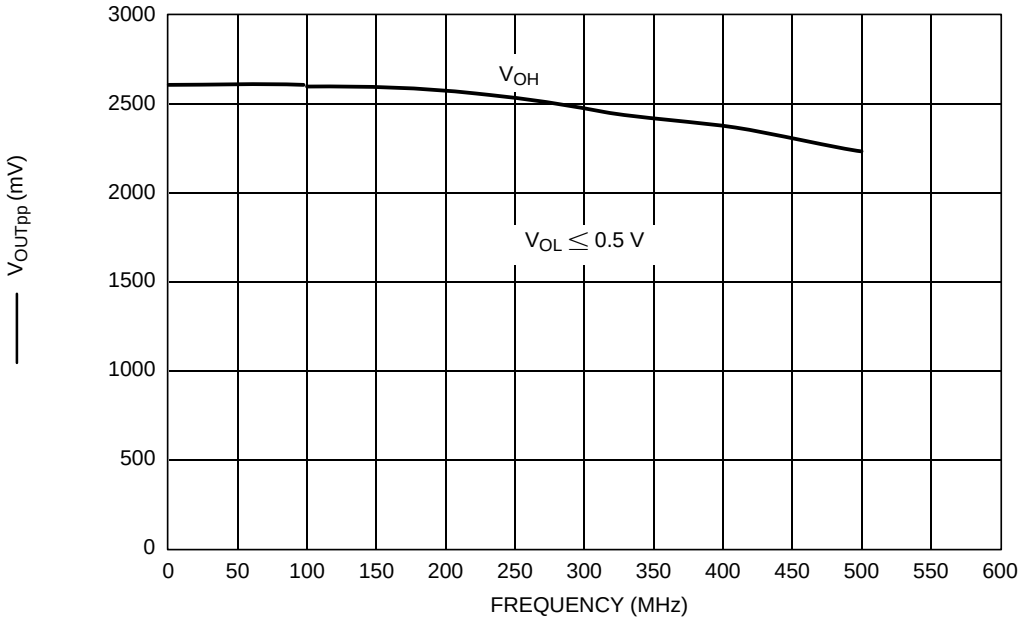


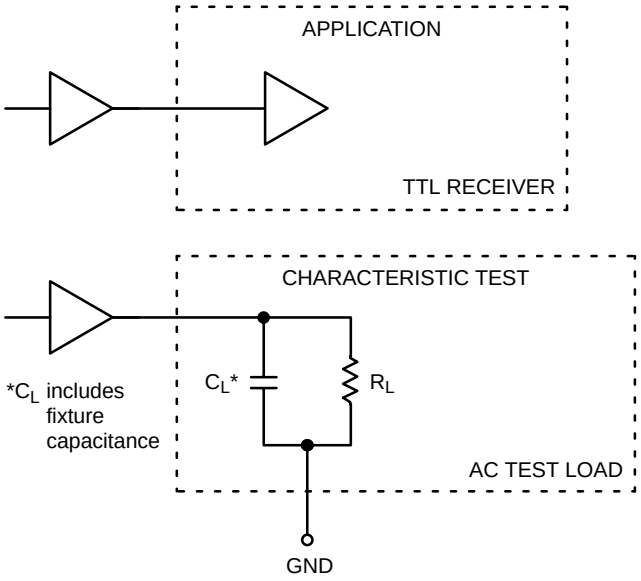
(Top View)

V_{CC}	PECL Power Supply	GND = 0 V		3.8	V
V_{IN}	PECL Input Voltage	GND = 0 V	$V_I \leq V_{CC}$	0 to 3.8	V
I_{BB}	V_{BB} Sink/Source			0.5	mA
T_A	Operating Temperature Range			−40 to +85	C
T_{stg}	Storage Temperature Range			−65 to +150	C
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm	SO−8 SO−8	190 130	C/W C/W q

V_{CC} = 3.3 V, GND = 0.0 V, T_A = −40 C to 85 C

V_{OH}	Output HIGH Voltage	I_{OH} = −3.0 mA	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA			0.5	V
I_{CCH}	Power Supply Current	Outputs set to HIGH	5	17	25	mA
I_{CCL}	Power Supply Current	Outputs set to LOW	8	21	30	mA
I_{OS}	Output Short Circuit Current		−130		−80	mA


3000
2500
2000
1500
1000
500
0
0
50
100
150
200
250
300
350
400
450
500
550
600
V_{OUTpp} (mV)
FREQUENCY (MHz)
V_{OH}
$V_{OL} \leq 0.5$ V

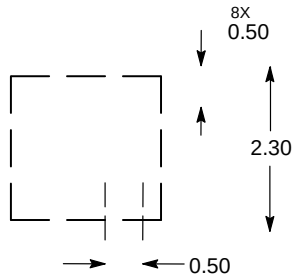

APPLICATION
TTL RECEIVER
CHARACTERISTIC TEST
*C_L includes fixture capacitance
C_L*
R_L
AC TEST LOAD
GND

DF 8 2□2, 0.5
CASE 506AA
ISSUE F

DATE 04 MAY 2016

1
CA E 4:1

DE I G F I *

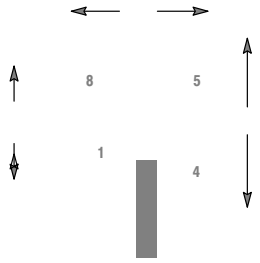


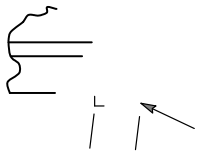
DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the m1 □ Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

SOIC 8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

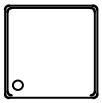


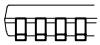


SEATING
PLANE

TSSOP−8 3.00x3.00x0.95
CASE 948R−02
ISSUE A

DATE 07 APR 2000





DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B				
