

MC100EPT22

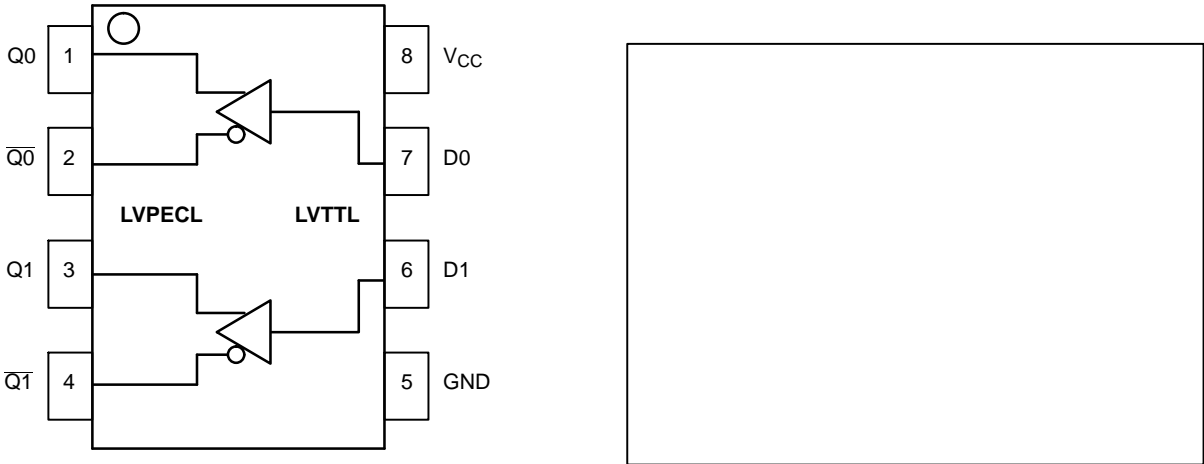


Figure 1. 8-Lead Pinout (Top View) and Logic Diagram

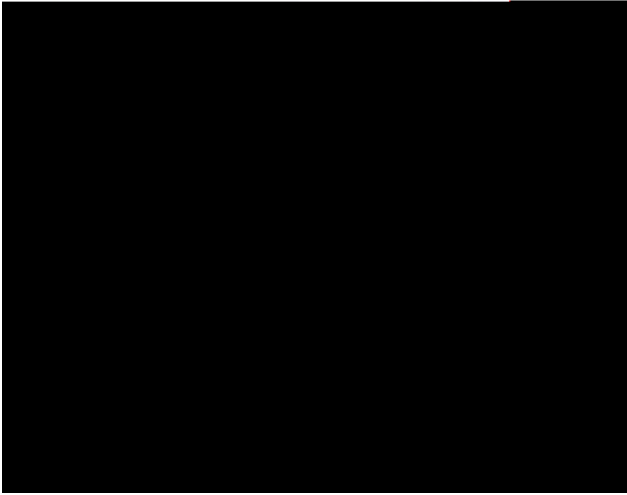


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Table 6. AC CHARACTERISTICS ($V_{CC} = 3.0\text{ V}$ to 3.6 V , $GND = 0.0\text{ V}$ (Note 5))

| Symbol | Characteristic | -40 C | | | 25 C | | | 85 C | | | Unit |
|-----------|------------------------------|-------|-----|-----|------|-----|-----|------|-----|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| f_{max} | Maximum Frequency (Figure 2) | 0.8 | | | | | | | | | |

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**Figure 3. Typical Phase Noise Plot at
 $f_{\text{carrier}} = 25 \text{ MHz}$**

The above phase noise plots captured using Agilent E5052A show additive phase noise of the MC100EPT22 device at frequencies 25 MHz and 156.25 MHz respectively at an operating voltage of 3.3 V in room temperature. The RMS Phase Jitter contributed by the device (integrated



**Figure 4. Typical Phase Noise Plot at
 $f_{\text{carrier}} = 156.25 \text{ MHz}$**

between 12 kHz and 20 MHz; as shown in the shaded region of the plot) at each of the frequencies is 158 fs and 48 fs respectively. The input source used for the phase noise measurements is Agilent E8663B.

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Resource Reference of Application Notes

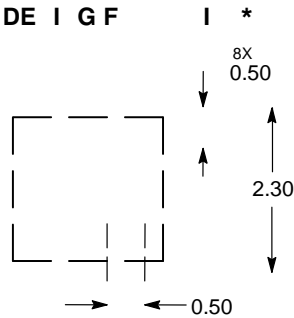
- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPiCE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

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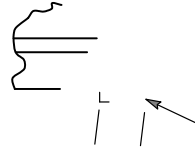
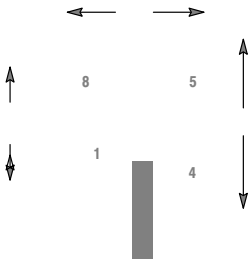


DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the [Soldering and Mounting Techniques Reference Manual, SOLDERRM/D](#).

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