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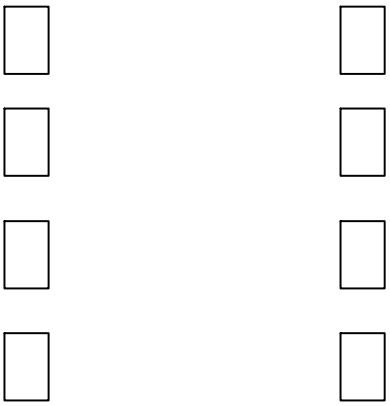
The MC100EPT25 is a Differential ECL to LVTTL translator. This device requires +3.3 V, ĭ3.3 V to ĭ5.2 V, and ground. The small outline 8ĭ



V_{CC}	Positive Power Supply	GND = 0 V	V_{EE} = −5.0 V	3.8	V
V_{EE}	Negative Power Supply	GND = 0 V	V_{CC} = +3.3 V	−6	V
V_{IN}	Input Voltage	GND = 0 V		0 to V_{EE}	V
I_{BB}	V_{BB} Sink/Source			0.5	mA
T_A	Operating Temperature Range			−40 to +85	C
T_{stg}	Storage Temperature Range			−65 to +150	C
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm	SOIC−8 NB	190 130	C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	Standard Board	SOIC−8 NB	41 to 44	C/W
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm	TSSOP−8	185 140	C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	Standard Board	TSSOP−8	41 to 44	C/W
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm	DFN−8	129 84	C/W
T_{sol}	Wave Solder (Pb−Free)	<2 to 3 sec @ 260 C		265	C
θ_{JC}	Thermal Resistance (Junction−to−Case)	(Note 2)	DFN−8	35 to 40	C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. JEDEC standard multilayer board − 2S2P (2 signal, 2 power)

(V_{CC} = 3.3 V; V_{EE} = −5.5 V to −3.0 V; GND = 0.0 V (Note 3))

		–									
IEE	Power Supply Current	8.0	16	25	8.0	16	25	8.0	16	25	mA
V_{IH}	Input HIGH Voltage Single−Ended	−1225		−880	−1225		−880	−1225		−880	mV
V_{IL}	Input LOW Voltage Single−Ended	−1945		−1625	−1945		−1625	−1945		−1625	mV
V_{BB}	Output Voltage Reference	−1525	−1425	−1325	−1525	−1425	−1325	−1525	−1425	−1325	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 4)	V_{EE} + 2.0		0.0	V_{EE} + 2.0		0.0	V_{EE} + 2.0		0.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

3. Input parameters vary 1:1 with GND.
4. V

(V_{CC} = 3.0 V to 3.6 V; V_{EE} = −5.5 V to −3.0 V; GND = 0.0 V (Note 5))

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- ECL Clock Distribution Techniques
- Designing with PECL (ECL at +5.0 V)
- ECLinPS™ I/O SPiCE Modeling Kit
- Metastability and the ECLinPS Family
- Interfacing Between LVDS and ECL
- The ECL Translator Guide
- Odd Number Counters Design
- Marking and Date Codes
- Termination of ECL Logic Devices
- Interfacing with ECLinPS
- AC Characteristics of ECL Devices

DF 8 2□2, 0.5
CASE 506AA
ISSUE F

DATE 04 MAY 2016

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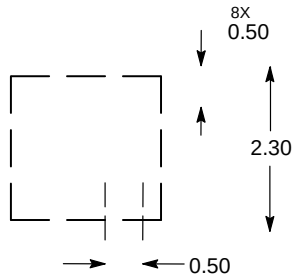

DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the m1 □ Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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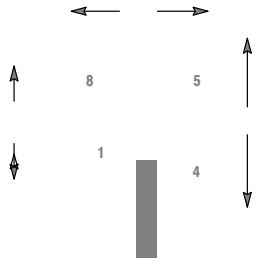
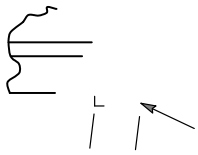
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

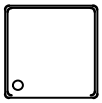


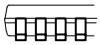


SEATING
PLANE

TSSOP 8 3.00x3.00x0.95
CASE 948R−02
ISSUE A

DATE 07 APR 2000





DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B				
