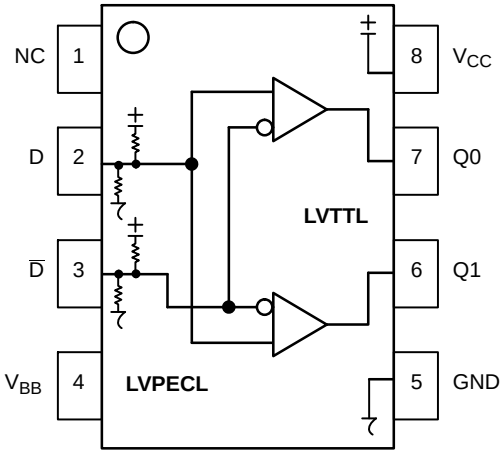

(Top View)

Figure 1. 8−Lead Pinout and Logic Diagram

Table 1. PIN DESCRIPTION

Pin	Function
Q0, Q1	LVTTL Outputs
D0**, D1**	Differential LVPECL Inputs Pair
V_{CC}	Positive Supply
V_{BB}	Output Reference Voltage
GND	Ground
NC	No Connect
EP	(DFN8 only) Thermal exposed pad must be connected to a sufficient thermal conduit. Electric-

Table 3. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating

Table 5. TTL OUTPUT DC CHARACTERISTICS (V_{CC} = 3.3 V; GND = 0.0 V; T_A = 40 C to 85 C)

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = 3.0 mA	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA			0.5	V
I_{CCH}	Power Supply Current		10	25	35	mA
I_{CCL}	Power Supply Current		15	34	40	mA
I_{OS}	Output Short Circuit Current		50		150	mA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit

DF 8 2□2, 0.5
CASE 506AA
ISSUE F

DATE 04 MAY 2016

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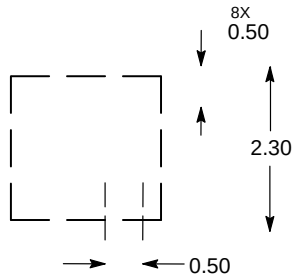

DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the m1 □ Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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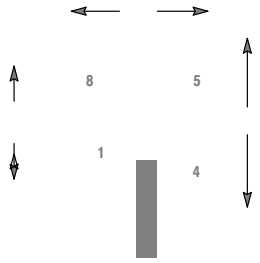
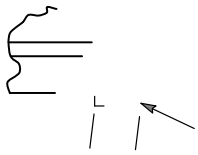
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

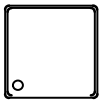


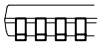


SEATING
PLANE

TSSOP 8 3.00x3.00x0.95
CASE 948R−02
ISSUE A

DATE 07 APR 2000





DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B				
