-Ac.4 1 FORMATION



Table 2. ATTRIBUTES

Characteristics	Value
Internal Input Pulldown Resistor	N/A
Internal Input Pullup Resistor	N/A
ESD Protection Human Body Model Machine Model Charged Device Model	> 2 kV > 150 V > 2 kV
Moisture Sensitivity, Indefinite Time Out of Drypack	Pb-Free Pkg
LQFP-32 QFN-32	Level 2 Level 1
Flammability Rating Oxygen Index: 28 to 34	UL 94 V–0 @ 0.125 in
Transistor Count	596 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	-

Table 3. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V _{CC}	Power Supply	V _{EE} = 0 V		5	V
VI	Input Voltage	V _{EE} = 0 V			

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Table 5. PECL INPUT DC CHARACTERISTICS V_{CC} = 3.3 V, GND= 0.0 V, T_A = -40° C to 85° C

Symbol	Characteristic	Condition	Min	Тур	Max	Unit
I _{IH}	Input HIGH Current	V _{IN} = 2420 mV			150	μΑ
IIL	Input LOW Current	V _{IN} = 1490 mV			200	μΑ
V _{IH}	Input HIGH Voltage		2075		2420	mV
V _{IL}	Input LOW Voltage		1490		1675	mV

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

Table 6. PECL OUTPUT DC CHARACTERISTICS $V_{CC} = 3.3 \text{ V}$, GND = 0.0 V (Note 1)

		-40°C		25°C			85°C				
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
I _{EE}	Power Supply Current	85	115	145	90	120	155	95	130	155	mA
V _{OH}	Output High Voltage (Note 2)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
V _{OL}	Output Low Voltage (Note 2)	1355	1520	1700	1355	1520	1700	1355	1520	1700	mV

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

1. Input and output parameters vary 1:1 with V_{CC} .

2. All loading with 50 Ω to V_{CC}–2.0 V.

Table 7. AC CHARACTERISTICS V_{CC} = 3.0 V to 3.8 V (Note 3)

		-40°C		25°C			85°C				
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
f _{max}	Maximum Frequency (See Figure 4)	1.0	1.5		1.0	1.5		1.0	1.5		GHz
t _{PLH} , t _{PHL}	Propagation Delay to Output (Figure 5, Note 4) D to Q ENPECL to Q ENTTL to Q	100 150 300	450 500 450	800 875 800	100 150 300	500 500 500	875 875 800	100 200 300	500 550 500	800 925 800	ps
t _{JITTER}	Random Clock Jitter (RMS) (See Figure 4)		0.7	3.0		0.7	3.0		0.7	3.0	ps
t _r / t _f	Output Rise/Fall Times (20% – 80%)	100	200	450	100	200	250	100	200	300	ps
T _{SKEW}	Duty Cycle Skew (Note 5) D to Q Channel 0–7 Channel 8–9 ENPECL to Q ENTTL to Q		120 200 120 100	375 775 400 275		120 200 120 100	375 775 400 275		120 200 120 100	375 775 400 275	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

3. Measured using a 2.4 V source, 50% duty cycle clock source. All loading with 50 Ω to V_{CC}-2.0 V.

4. 1.5 V to 50% point of the output. 5. Duty cycle skew $|t_{PLH} - t_{PHL}|$ on the specific path.

MC100EPT622

ORDERING INFORMATION

Device	Package	Shipping
MC100EPT622FAG	LQFP–32 (Pb–Free)	250 Units / Tray
MC100EPT622MNG	QFN32 (Pb-Free)	74 Units / Rail

Resource Reference of Application Notes

AN1405/D	-	ECL Clock Distribution Techniques
AN1406/D	-	Designing with PECL (ECL at +5.0 V)
AN1503/D	_	ECLinPS [™] I/O SPiCE Modeling Kit
AN1504/D	_	Metastability and the ECLinPS Family
AN1568/D	-	Interfacing Between LVDS and ECL
AN1672/D	_	The ECL Translator Guide
AND8001/D	-	Odd Number Counters Design
AND8002/D	_	Marking and Date Codes
AND8020/D	-	Termination of ECL Logic Devices
AND8066/D	_	Interfacing with ECLinPS
AND8090/D	_	AC Characteristics of ECL Devices

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DIMENSION: MILLIMETERS

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