D0−D3	ECL Data Inputs
Q, $\overline{Q}$	ECL Data Outputs
V_{CCS}	

(V_{CC} = 3.3 V; V_{EE} = 0 V (Note 1))

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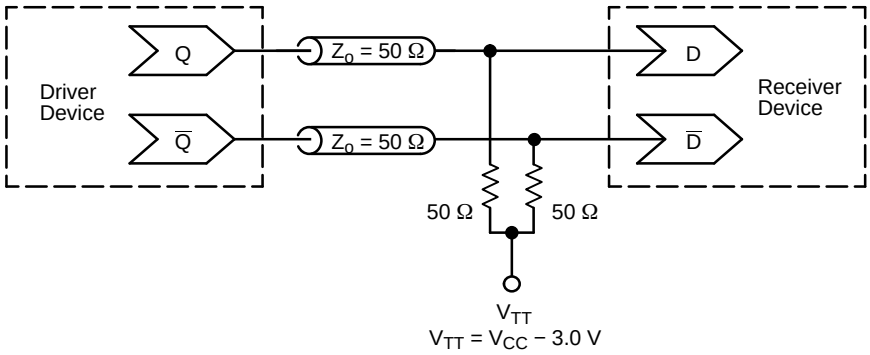

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- ECL Clock Distribution Techniques
- Designing with PECL (ECL at +5.0 V)
- ECLinPS™ I/O SPiCE Modeling Kit
- Metastability and the ECLinPS Family
- Interfacing Between LVDS and ECL
- The ECL Translator Guide
- Odd Number Counters Design
- Marking and Date Codes
- Termination of ECL Logic Devices
- Interfacing with ECLinPS
- AC Characteristics of ECL Devices

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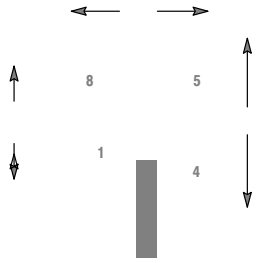

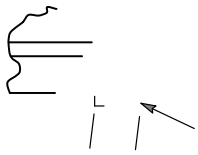

SEATING
PLANE