

3.3 V ECL 2-Input Differential AND/NAND

MC100LVEL05

Description

The MC100LVEL05 is a 2-input differential AND/NAND gate. The device is functionally equivalent to the MC100EL05 device and operates from a 3.3 V supply voltage. With propagation delays and output transition times equivalent to the EL05, the LVEL05 is ideally suited for those applications which require the ultimate in AC performance at low voltage power supplies.

Because a negative 2-input NAND is equivalent to a 2-input OR function, the differential inputs and outputs of the device allows the LVEL05 to also be used as a 2-input differential OR/NOR gate.

Features

340 ps Propagation Delay

High Bandwidth Output Transitions

ESD Protection:

> 4 kV Human Body Mode

> 200 V Machine Model

The 100 Series Contains Temperature Compensation

PECL Mode Operating Range: $V_{CC} = 3.0 \text{ V}$ to 3.8 V

with $V_{EE} = 0 V$

NECL Mode Operating Range: $V_{CC} = 0 \text{ V}$

with $V_{EE} = 3.0 \text{ V}$ to 3.8 V

Internal Input Pulldown Resistors

Q Output will Default LOW with All Inputs Open or at VEE

Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test

Moisture Sensitivity

Level 1 for SOIC 8

Level 3 for TSSOP 8

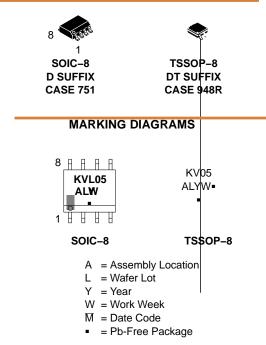
For Additional Information, see Application Note AND8003/D

Flammability Rating: UL 94 V 0 @ 0.125 in,

Oxygen Index: 28 to 34

Transistor Count = 69 Devices

These Devices are Pb-Free, Halogen Free and are RoHS Compliant



*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

Device	Package	Shipping [†]
MC100LVEL05DG	SOIC-8 (Pb-Free)	98 Units/Tube
MC100LVEL05DR2G	SOIC-8 (Pb-Free)	2500/Tape & Reel
MC100LVEL05DTR2G	TSSOP-8 (Pb-Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MC100LVEL05

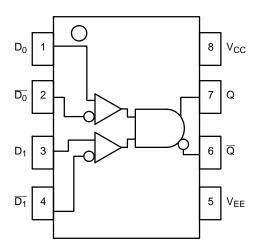


Figure 1. Logic Diagram and Pinout Assignment

Table 1. PIN DESCRIPTION

PIN	FUNCTION
D0, $\overline{\text{D0}}$; D1, $\overline{\text{D1}}$ Q, $\overline{\text{Q}}$ V _{CC} V _{EE}	ECL Data Inputs ECL Data Outputs Positive Supply Negative Supply

Table 2. MAXIMUM RATINGS

MC100LVEL05

Table 3. LVPECL DC CHARACTERISTICS ($V_{CC} = 3.3 \text{ V}; V_{EE} = 0.0 \text{ V} \text{ (Note 1))}$

			-40 C	25 C	85 C	
Symbol	Characteristic	Min	Тур			

MC100LVEL05

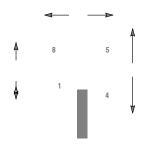
 $\textbf{Table 5. AC CHARACTERISTICS} \ (\text{V}_{CC} = 3.3 \ \text{V}; \ \text{V}_{EE} = 0.0 \ \text{V} \ \text{or} \ \text{V}_{CC} = 0.0 \ \text{V}; \ \text{V}_{EE} = -3.3 \ \text{V} \ (\text{Note 1}))$

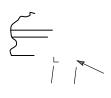
			-40°C			25 C			85 C		
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
f _{max}	Maximum Toggle Frequency		1.6			1.6			1.6		GHz
t _{PLH} t _{PHL}	Propagation Delay to Output	240	260	440	240	340	440	250		450	ps
t _{JITTER}	Cycle-to-Cycle Jitter		6.7			7.5			8.2		ps

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SOIC 8 NB CASE 751-07 ISSUE AK

DATE 16 FEB 2011





SEATING PLANE



TSSOP 8 3.00x3.00x0.95 CASE 948R-02

CASE 948R-02 ISSUE A

DATE 07 APR 2000





	MILLIN	IETERS	INCHES			
DIM	MIN	MAX	MIN	MAX		
Α	2.0	3.10	0.114	0.122		
В						

