(V_{CC} = 3.3 V; V_{EE} = 0.0 V (Note 1))

		– °			°			°			
I_{EE}	Power Supply Current		30	35		30	35		32	38	mA
V_{OH}	Output HIGH Voltage (Note 2)	2215	2295	2420	2275	2345	2420	2275	2345	2420	mV
V_{OL}	Output LOW Voltage (Note 2)	1470	1605	1745	1490	1595	1680	1490	1595	1680	mV
V_{IH}	Input HIGH Voltage	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage	1490		1825	1490		1825	1490		1825	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
2. Outputs are terminated through a 50 Ω resistor to V_{CC} − 2.0 V.

(V_{CC} = 0.0 V; V_{EE} = −3.3 V (Note 1))

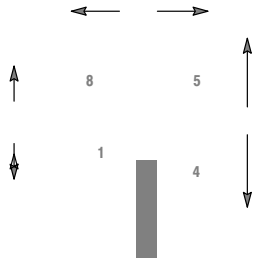
		– °			°			°			
I_{EE}	Power Supply Current		30	35		30	35		32	38	mA
V_{OH}	Output HIGH Voltage (Note 2)	−1085	−1005	−880	−1025	−955	−880	−1025	−955	−880	mV
						−1705	−1620	−1810	−1705	−1620	mV
							−880	−1165		−880	mV
							−1475	−1810			

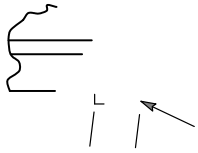
(V_{CC} = 3.3 V; V_{EE} = 0.0 V or V_{CC} = 0.0 V; V_{EE} = −3.3 V (Note 1))

		– °			°			°			
f_{max}	Maximum Toggle Frequency	2.7			2.9			2.9			GHz
t_{PLH} t_{PHL}	Propagation Delay to Output CLK S, R	 365 385	 465 475	 580 620	 375 395	 475 485	 590 630	 415 435	 530 525	 630 670	ps
t_S t_H	Setup Time Hold Time	150 250	0 100		150 250	0 100		150 250	0 100		ps
t_{RR}	Set/Reset Recovery	400	200		400	200		400	200		ps
t_{JITTER}	Cycle-to-Cycle Jitter		6.9			7.0			7.1		ps
t_{PW}	Minimum Pulse Width CLK Set, Reset	 340 600			 340 600			 340 600			ps
t_r t_f	Output Rise / Fall Times Q (20%										

SOIC 8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

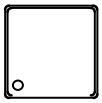


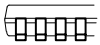


SEATING
PLANE

TSSOP 8 3.00x3.00x0.95
CASE 948R−02
ISSUE A

DATE 07 APR 2000





DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B				
