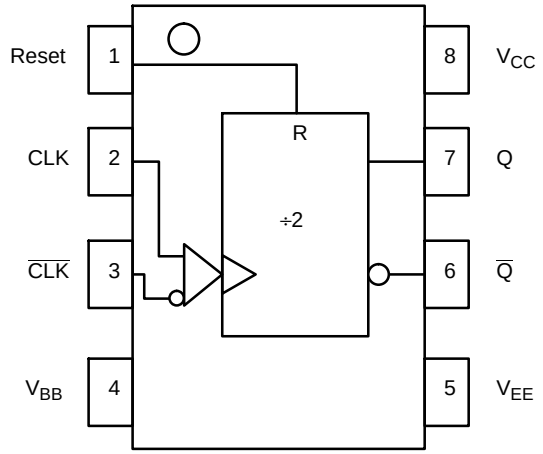

Figure 1. Logic Diagram and Pinout Assessment

Table 1. PIN DESCRIPTION

Pin	Function
CLK*, $\overline{CLK}$**	ECL Differential Clock Inputs
Q, $\overline{Q}$	ECL Differential Data ÷2 Outputs
Reset*	ECL Asynch Reset
V_{BB}	Reference Voltage Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply

*Pin will default low when left open, per internal 75 K pull-down to V_{EE}.
** Pin will default to $V_{CC}/2$ when left open per internal 75 KΩ pull-down to V_{EE} and 75 KΩ pull-up to V_{CC}.

Table 2. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}					

Table 3. LVPECL DC CHARACTERISTICS (V_{CC} = 3.3 V; V_{EE} = 0.0 V (Note 1))

Symbol	Characteristic	−40°C	25°C	85°C	Unit

Table 5. AC CHARACTERISTICS (V_{CC} = 3.3 V; V_{EE} = 0.0 V or V_{CC} = 0.0 V; V_{EE} = 3.3 V (Note 1))

		−40°C			25°C		85°C	
Symbol	Characteristic	Min	Typ	Max	Min	TypMax		Unit

Resource Reference of Application Notes

AN1405/D	ECL Clock Distribution Techniques
AN1406/D	Designing with PECL (ECL at +5.0 V)
AN1503/D	ECLinPS I/O SPiCE Modeling Kit
AN1504/D	Metastability and the ECLinPS Family
AN1568/D	Interfacing Between LVDS and ECL
AN1672/D	The ECL Translator Guide
AND8001/D	Odd Number Counters Design
AND8002/D	Marking and Date Codes
AND8020/D	Termination of ECL Logic Devices
AND8066/D	Interfacing with ECLinPS
AND8090/D	AC Characteristics of ECL Devices

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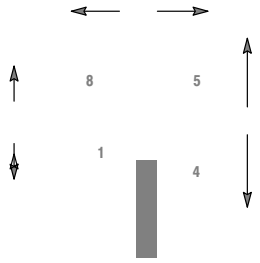
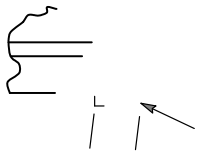
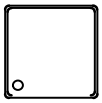


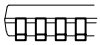


SEATING
PLANE

TSSOP 8 3.00x3.00x0.95
CASE 948R−02
ISSUE A

DATE 07 APR 2000





DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B				
