3.3 V ECL 4 Divider

MC100LVEL33

8 ‘

1

SOIC−8 NB
D SUFFIX
CASE 751−07

MARKING DIAGRAMS*

KV33
ALYW▪
▪

Description

µ

Features

*For additional marking information, refer to Application Note AND8002/D.

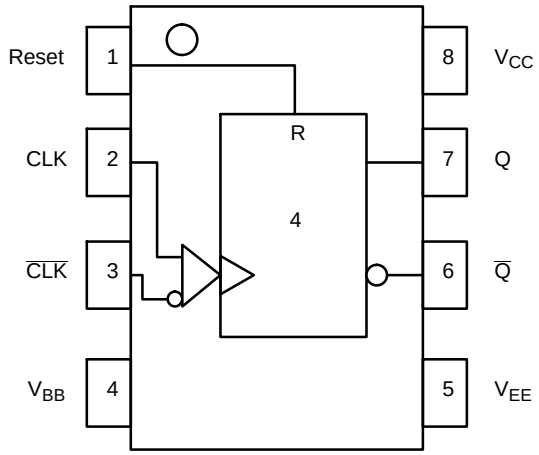

Figure 1. Logic Diagram and Pinout Assignment

Table 1. PIN DESCRIPTION

PIN	FUNCTION
CLK*, $\overline{CLK}$**	ECL Differential Clock Inputs
Q, $\overline{Q}$	ECL Differential Data 4 Outputs
Reset*	ECL Asynch Reset
V_{BB}	Reference Voltage Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply

* Pins will default LOW when open due to internal 75 kΩ resistor to V_{EE}

** Pins will default to 1/2 V_{CC} when open due to internal resistors: 75 kΩ to V_{EE} and 75 kΩ to V_{CC}

Table 2. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8 to 0	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		−8 to 0	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	V_I V_{CC} V_I V_{EE}	6 to 0 −6 to 0	V
I_{out}	Output Current	Continuous Surge		50 100	mA
I_{BB}	V_{BB} Sink/Source			0.5	mA
T_A	Operating Temperature Range			−40 to +85	C
T_{stg}	Storage Temperature Range			−65 to +150	C
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	SOIC−8 NB SOIC−8 NB	190 130	C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	SOIC−8 NB	41 to 44 5%	C/W
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	TSSOP−8 TSSOP−8	185 140	C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	TSSOP−8		

Table 3. LVPECL DC CHARACTERISTICS (V_{CC} = 3.3 V; V_{EE} = 0.0 V (Note 1))

Symbol	Characteristic	−40 C			25 C			85 C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		33	37		33	37		35	39	mA
V_{OH}	Output HIGH Voltage (Note 2)	2215	2295	2420	2275	2345	2420	2275	2345	2420	mV
V_{OL}	Output LOW Voltage (Note 2)-	1470	1605	1745	1490	1595	1680	1490	1595	1680	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage (Single-Ended)	1490		1825	1490		1825	1490		1825	mV
V_{BB}	Output Voltage Reference	1.92		2.04	1.92		2.04	1.92		2.04	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3) V_{PP} 500 Mv V_{PP} 500 mV	 1.2 1.4		 2.9 2.9	 1.1 1.3		 2.9 2.9	 1.1 1.3		 2.9 2.9	V
I	Input HIGH Current			150							

Table 5. AC CHARACTERISTICS (V_{CC} = 3.3 V; V_{EE} = 0.0 V or V_{CC} = 0.0 V; V_{EE} = −3.3 V (Note 1))

Symbol	Characteristic	−40 C			25 C			85 C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency	3.4			3.8	4.0		3.8			GHz
t_{PLH} t_{PHL}	Propagation Delay CLK to Q (Diff) CLK to Q (SE) Reset to Q	 530 530 500	 630 655	 730 780 700	 570 570 520	 670 695	 770 820 720	 650 650 580	 750 775	 850 900 780	 ps
t_{RR}	Reset Recovery	300			300			300			ps

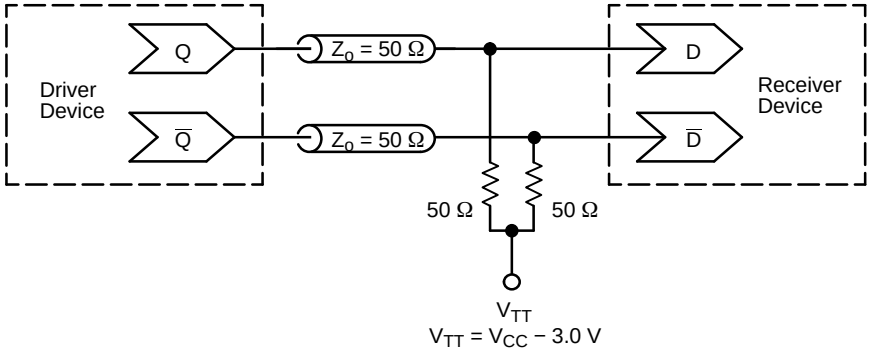

Figure 2. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D − Termination of ECL Logic Devices)

Resource Reference of Application Notes

AN1405/D − ECL Clock Distribution Techniques
AN1406/D − Designing with PECL (ECL at +5.0 V)
AN1503/D − ECLinPS™ I/O SPiCE Modeling Kit
AN1504/D − Metastability and the ECLinPS Family
AN1568/D − Interfacing Between LVDS and ECL
AN1672/D − The ECL Translator Guide
AND8001/D − Odd Number Counters Design
AND8002/D − Marking and Date Codes
AND8020/D − Termination of ECL Logic Devices
AND8066/D − Interfacing with ECLinPS
AND8090/D − AC Characteristics of ECL Devices

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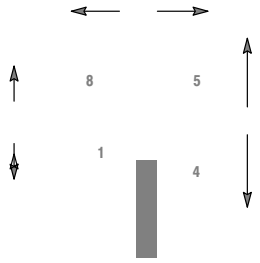
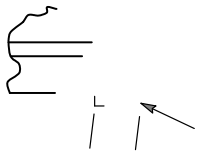
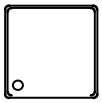


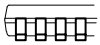


SEATING
PLANE

TSSOP 8 3.00x3.00x0.95
CASE 948R−02
ISSUE A

DATE 07 APR 2000





DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B				
