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DATA SHEET



Warning: All $V_{\mbox{CC}}$ and $V_{\mbox{EE}}$ pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. 16 Lead Pinout (Top View) and Logic Diagram

Table 3. ATTRIBUTES

Characteristics

Table 1. PIN DESCRIPTION

PIN	FUNCTION
CLK*, CLK**	ECL Diff Clock Inputs
ĒN*	ECL Sync Enable
MR*	ECL Master Reset
Q0, <u>Q0</u>	ECL Diff 2 Outputs
Q1, <u>Q1</u>	ECL Diff 4 Outputs
Q2, <u>Q2</u>	ECL Diff 8 Outputs
V _{BB}	Reference Voltage Output
V _{CC}	Positive Supply
V _{EE}	Negative Supply
NC	No Connect

* Pins will default LOW when left open.

***Pins will default to $V_{CC}/2$ when left open.

Table 2. FUNCTION TABLE

CLK	EN	MR	FUNCTION
Z ZZ X	L H X	LLH	Divide Hold Q ₀₋₃ Reset Q ₀₋₃

Z = Low-to-High Transition ZZ = High-to-Low Transition

Value

MC100LVEL34

Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V _{CC}	PECL Mode Power Supply	$V_{EE} = 0 V$		6	V
V_{EE}	NECL Mode Power Supply	$V_{CC} = 0 V$		-6	V
VI	1	-	-	-	-

MC100LVEL34

MC100LVEL34



Figure 5. Typical Termination for Output Driver and Device Evaluation (See Application Note <u>AND8020/D</u> Termination of ECL Logic Devices.)



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- DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
 MAXIMUM MOLD PROTRUSION 0.1^r

b DIMENSION AT MAXIMUM MATE

nm TOTAL IN EXCESS OF THE



<u>top view</u>

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GENERIC MARKING DIAGRAM*

16	H	- A	H.	H	H	H.	H.	E
		XX)	(X)	XX	(X)	XX	(XC	3
		XXX	(X)	XX)	XX	XX)	(X)	<
	0		A١	NĽ	ΥW	W		
		<u> </u>						
1	н	н	н	н	н	н	н	Н

XXXXX = Specific Device Code

A = Assembly Location

- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.



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