

# MC100LVELT20

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## 3.3 V LVTTTL/LVCMOS to Differential LVPECL Translator

### Description

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### Features

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### MARKING DIAGRAM

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- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

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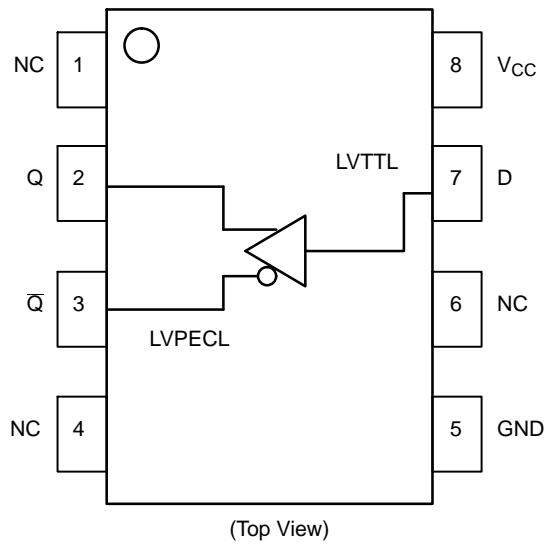


Figure 1. 8-Lead Pinout and Logic Diagram

Table 1. PIN DESCRIPTION

| Pin             | Function                  |
|-----------------|---------------------------|
| Q, $\bar{Q}$    | Differential PECL Outputs |
| D               | LVTTTL Input              |
| V <sub>CC</sub> | Positive Supply           |
| GND             | Ground                    |
| NC              | No Connect                |

Table 2. ATTRIBUTES

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**Table 4. LVTTTL INPUT DC CHARACTERISTICS** ( $V_{CC} = 3.3\text{ V}$ ,  $GND = 0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

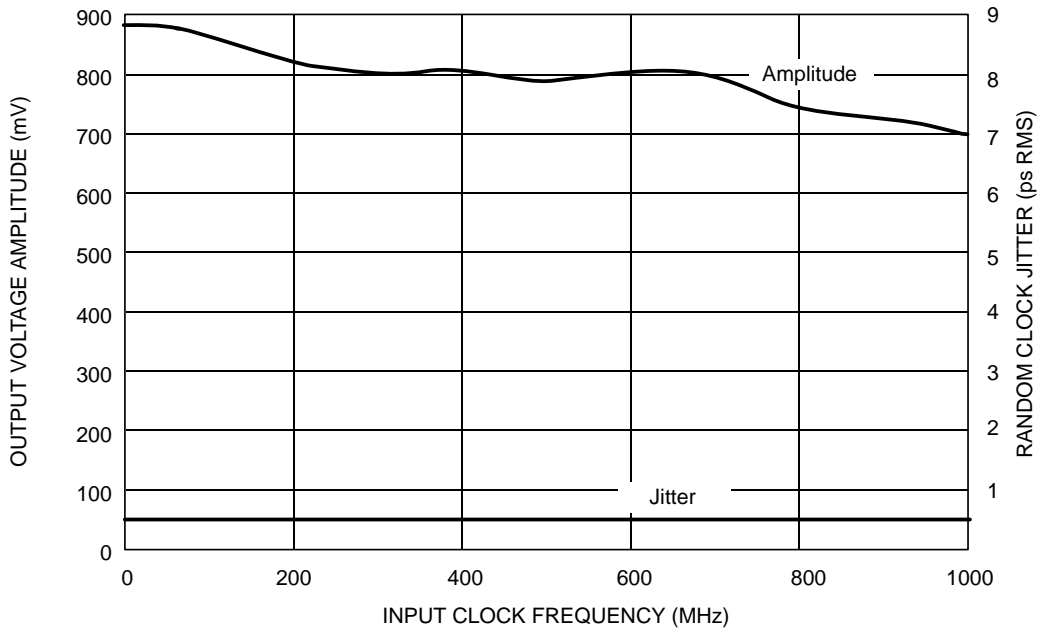
| Symbol    | Characteristic                                     | Min | Typ | Max  | Unit          |
|-----------|--|-----|-----|------|---------------|
| $I_{IH}$  | Input HIGH Current ( $V_{in} = 2.7\text{ V}$ )     |     |     | 20   | $\mu\text{A}$ |
| $I_{IHH}$ | Input HIGH Current MAX ( $V_{in} = 6.0\text{ V}$ ) |     |     | 100  | $\mu\text{A}$ |
| $I_{IL}$  | Input LOW Current ( $V_{in} = 0.5\text{ V}$ )      |     |     | -0.6 | $\text{mA}$   |
| $V_{IK}$  | Input Clamp Voltage ( $I_{in} = -18\text{ mA}$ )   |     |     | -1.2 | $\text{V}$    |
| $V_{IH}$  | Input HIGH Voltage                                 | 2.0 |     |      | $\text{V}$    |
| $V_{IL}$  | Input LOW Voltage                                  |     |     | 0.8  | $\text{V}$    |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

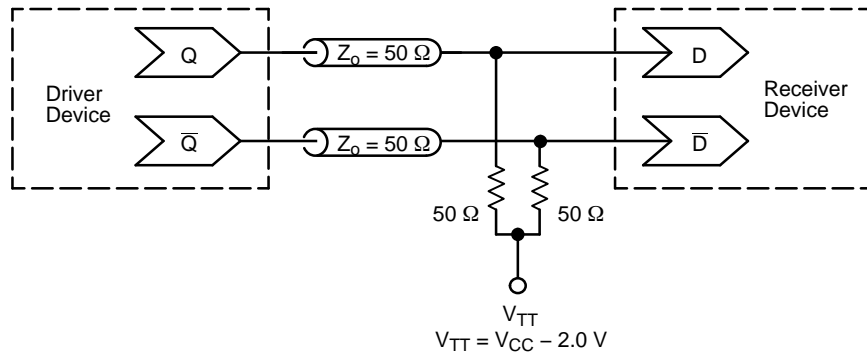
**Table 5. 100LVELT PECL OUTPUT DC CHARACTERISTICS** ( $V_{CC} = 3.3\text{ V}$ ,  $GND = 0\text{ V}$  (Note 1))

| Symbol   | Characteristic                | $-40^\circ\text{C}$ |      |      | $25^\circ\text{C}$ |     |     | $85^\circ\text{C}$ |     |     | Unit        |
|----------|-------------------------------|---------------------|------|------|--------------------|-----|-----|--------------------|-----|-----|-------------|
|          |                               | Min                 | Typ  | Max  | Min                | Typ | Max | Min                | Typ | Max |             |
| $I_{CC}$ | Negative Power Supply Current | 20                  | 25   | 30   | 22                 | 27  | 32  | 23                 | 28  | 33  | $\text{mA}$ |
| $V_{OH}$ | Output HIGH Voltage (Note 2)  | 2155                | 2280 | 2405 |                    |     |     |                    |     |     |             |

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**Figure 2. Output Voltage Amplitude ( $V_{OUTpp}$ )/RMS Jitter vs. Input Clock Frequency at Ambient Temperature**



**Figure 3. Typical Termination for Output Driver and Device Evaluation (See Application Note [AND8020/D](#) – Termination of ECL Logic Devices.)**

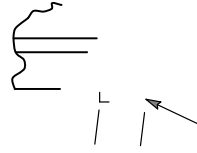
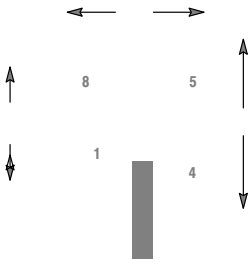
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## Resource Reference of Application Notes

AN1405/D – ECL Clock Distribution Techniques AN1465/D

**SOIC 8 NB**  
CASE 751-07  
ISSUE AK

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SEATING  
PLANE





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