3.3 V D V L V L/L V CMOS L V PECL

MC100L V EL 22

Description

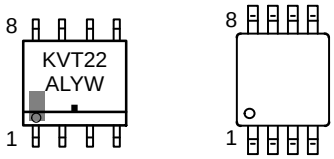
The MC100LVELT22 is a dual LVTTL/LVCMOS to differential LVPECL translator. Due to LVPECL (Low Voltage Positive ECL) levels, only +3.3V and ground is required. The small 8 ǐ lead package outline with low skew dual gate design makes the MC100LVELT22 ideal for applications which require translation of a clock and/or data signal.

Features

350 ps Typical Propagation Delay

<100 ps Output ǐ to ǐ

MARKING DIAGRAM



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

Device	Package	Shipping†
MC100LVELT22DG	SOIC−8 (Pb-Free)	98 Units / Tube
MC100LVELT22DR2G	SOIC−8 (Pb-Free)	2500Tape & Reel
MC100LVELT22DTG	TSSOP−8 (Pb-Free)	100 Units / Tube
MC100LVELT22DTRG	TSSOP−8 (Pb-Free)	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

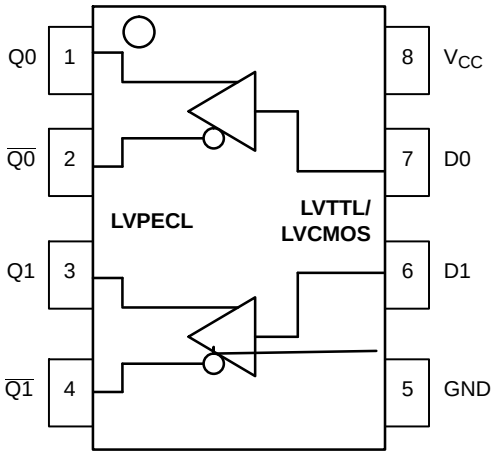


Figure 1. 8 Lead Pinout (Top View) **and Logic Diagram**

Table 1. PIN DESCRIPTION

PIN	FUNCTION
Qn, $\overline{Qn}$	LVPECL Differential Outputs

Table 4. LVPECL DC CHARACTERISTICS V_{CC} = 3.3 V; GND = 0.0 V (Note 3)

Symbol	Characteristic	40 C			25 C			85 C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{CC}	Power Supply Current			28			28			29	mA
V_{OH}	Output HIGH Voltage (Note 4)	2275		2420	2275		2420	2275		2420	mV
										1680	mV

ocket or printed circuit

Condition
V_{IN} = 2.7 V
V_{IN} = V_{CC}
V_{IN} = 0.5 V
$_{IN}$ = −18 mA

ocket or printed circuit

MC100LVELT22

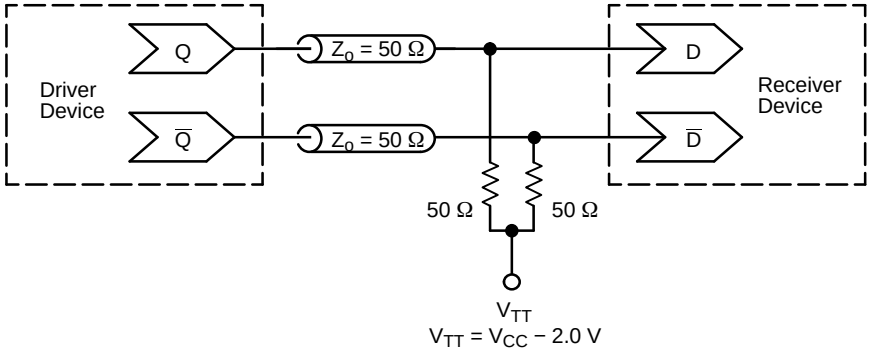


Figure 3. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1405/D	−	ECL Clock Distribution Techniques
AN1406/D	−	Designing with PECL (ECL at +5.0 V)
AN1503/D	−	ECLinPS™ I/O SPiCE Modeling Kit
AN1504/D	−	Metastability and the ECLinPS Family
AN1568/D	−	Interfacing Between LVDS and ECL
AN1672/D	−	The ECL Translator Guide
AND8001/D	−	Odd Number Counters Design
AND8002/D	−	Marking and Date Codes
AND8020/D	−	Termination of ECL Logic Devices
AND8066/D	−	Interfacing with ECLinPS
AND8090/D	−	AC Characteristics of ECL Devices

SOIC 8 NB
CASE 751−07
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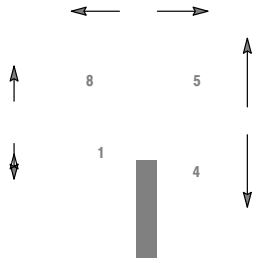
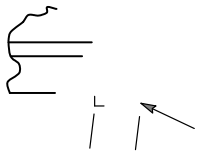
DATE 16 FEB 2011

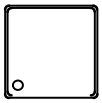


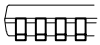


SEATING
PLANE

TSSOP 8 3.00x3.00x0.95
CASE 948R−02
ISSUE A

DATE 07 APR 2000





DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B				
