

3.3V D L L/L CMOS L/PECL



MC100LVELT22

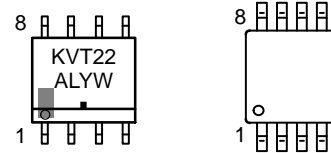
Description

The MC100LVELT22 is a dual LVTTTL/LVCMOS to differential LVPECL translator. Due to LVPECL (Low Voltage Positive ECL) levels, only +3.3V and ground is required. The small 8 lead package outline with low skew dual gate design makes the MC100LVELT22 ideal for applications which require translation of a clock and/or data signal.

Features

- 350 ps Typical Propagation Delay
- <100 ps Output to

MARKING DIAGRAM



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- M̄ = Date Code
- = Pb-Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note [AND8002/D](#).

ORDERING INFORMATION

Device	Package	Shipping†
MC100LVELT22DG	SOIC-8 (Pb-Free)	98 Units / Tube
MC100LVELT22DR2G	SOIC-8 (Pb-Free)	2500Tape & Reel
MC100LVELT22DTG	TSSOP-8 (Pb-Free)	100 Units / Tube
MC100LVELT22DTRG	TSSOP-8 (Pb-Free)	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

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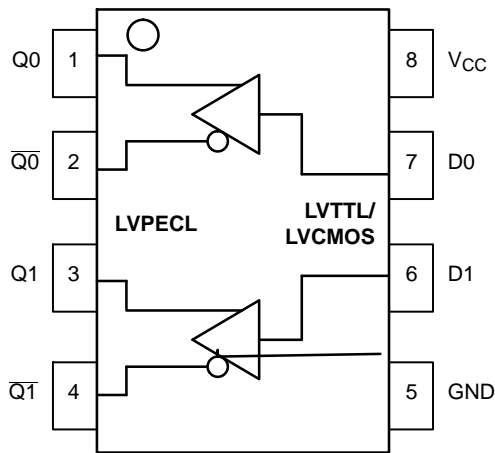


Table 1. PIN DESCRIPTION

PIN	FUNCTION
Qn, \overline{Qn}	LVPECL Differential Outputs

Figure 1. 8 Lead Pinout (Top View) and Logic Diagram

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Table 4. LVPECL DC CHARACTERISTICS $V_{CC} = 3.3\text{ V}$; $GND = 0.0\text{ V}$ (Note 3)

Symbol	Characteristic	40 C			25 C			85 C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{CC}	Power Supply Current			28			28			29	mA
V_{OH}	Output HIGH Voltage (Note 4)	2275		2420	2275		2420	2275		2420	mV
										1680	mV

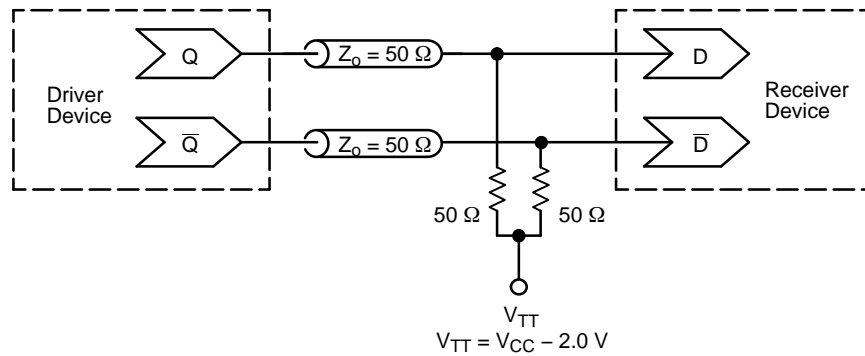
socket or printed circuit

Condition
$V_{IN} = 2.7\text{ V}$
$V_{IN} = V_{CC}$
$V_{IN} = 0.5\text{ V}$
$I_{IN} = -18\text{ mA}$

socket or printed circuit

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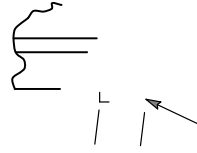
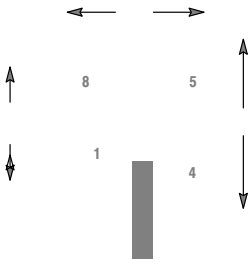
**Figure 3. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020/D Termination of ECL Logic Devices.)**

Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPICE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

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PLANE



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