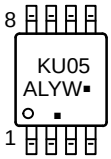
2.5 V/3.3 V ECL 2-Input Differential AND/NAND

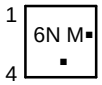
MC100LVEP05

The MC100LVEP05 is a 2−input differential AND/NAND gate. The MC100LVEP05 is the low voltage version of the MC100EP05 and is functionally equivalent to the EL05 and LVEL05 devices. With AC performance much faster than the LVEL05 device, the MC100LVEP05 is ideal for low voltage applications requiring the fastest AC performance available.

The 100 Series contains temperature compensation.

- 220 ps Typical Propagation Delay
- Input Clock Frequency > 3 GHz
- 0.2 ps Typical RMS Random Clock Period Jitter
- LVPECL Mode Operating Range: V_{CC} = 2.375 V to 3.6 V with V_{EE} = 0 V
- NECL Mode Operating Range: V_{CC} = 0 V with V_{EE} = −2.375 V to −3.6 V
- Open Input Default State
- Q Output Will Default LOW with Inputs Open
- These Device are Pb−Free, Halogen Free and are RoHS Compliant





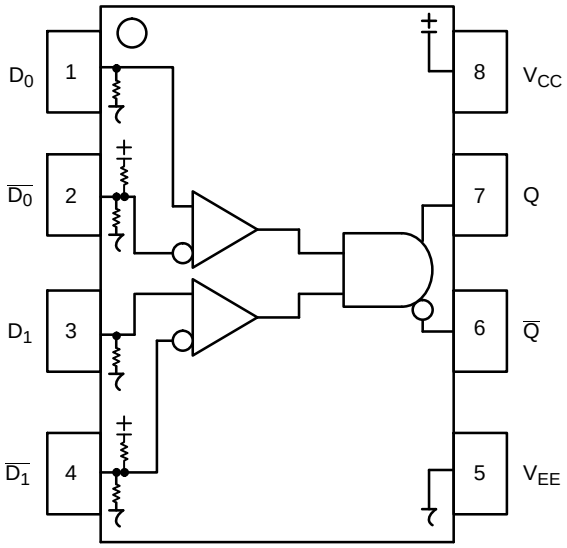
K = MC100
M = Date Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

		†
MC100LVEP05DTG	TSSOP−8 (Pb−Free)	100 Units / Tube
MC100LVEP05DTR2G	TSSOP−8 (Pb−Free)	2500 / Tape & Reel
MC100LVEP05MNTXG	DFN8 (Pb−Free)	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



(Top View)

D0*, D1*, D0**, D1**	ECL Data Inputs
Q, Q	ECL Data Outputs
V_{CC}	Positive Supply
V_{EE}	Negative Supply
EP	

V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		6	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		−6	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \le V_{CC}$ $V_I \ge V_{EE}$	6 −6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
T_A	Operating Temperature Range			−40 to +85	C
T_{stg}	Storage Temperature Range			−65 to +150	C
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm	TSSOP−8 TSSOP−8	185 140	C/W C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	Standard Board	TSSOP−8	41 to 44	C/W
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm	DFN8 DFN8	129 84	C/W C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	(Note 2)	DFN8	35 to 40	

V_{CC} = 3.3 V, V_{EE} = 0 V (Note 7)

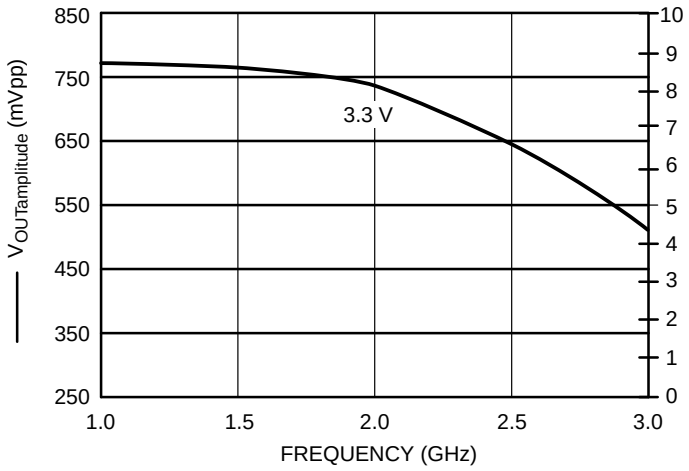
		–									
I_{EE}	Power Supply Current	15	25	32	17						

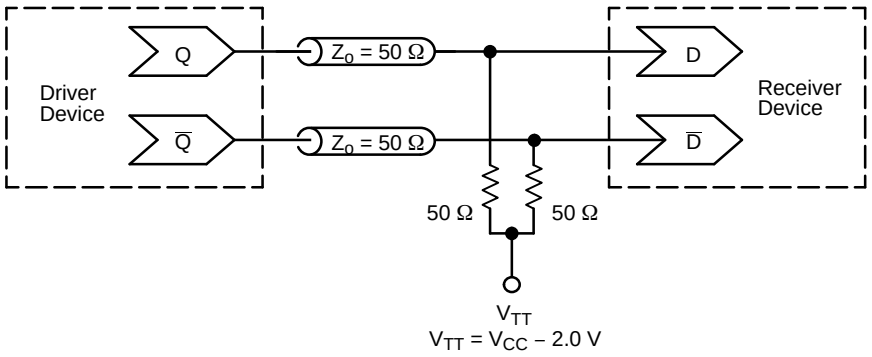
V_{CC} = 0 V; V_{EE} = −2.375 V to −3.6 V or V_{CC} = 2.375 V to 3.6 V; V_{EE} = 0 V (Note 13)

		–									
f_{max}	Maximum Frequency (Figure 2)	3.0			3.0			3.0			GHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential	160	210	260	170	220	270	210	260	320	ps
t_{JITTER}	RMS Random Clock Jitter $f_{in} \leq$ 3.0 GHz (Figure 2)		0.2	1		0.2	1		0.2	1.5	ps
V_{PP}	Input Voltage Swing (Differential Configuration)	150	800	1200	150	800	1200	150	800	1200	mV
t_r t_f	Output Rise/Fall Times (20% – 80%) Q	70	120	170	80	130	180	100	150	200	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

13. Measured using a 750 mV source, 50% duty cycle clock source. All loading with 50 Ω to V_{CC} − 2.0 V.





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- ECL Clock Distribution Techniques
- Designing with PECL (ECL at +5.0 V)
- ECLinPS™ I/O SPiCE Modeling Kit
- Metastability and the ECLinPS Family
- Interfacing Between LVDS and ECL
- The ECL Translator Guide
- Odd Number Counters Design
- Marking and Date Codes
- Termination of ECL Logic Devices
- Interfacing with ECLinPS
- AC Characteristics of ECL Devices

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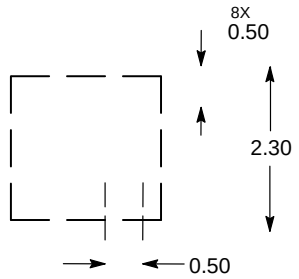

DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the m1 □ Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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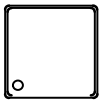
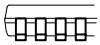
CASE 948R−02
ISSUE A

DATE 07 APR 2000





DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B				
